产 品 规 格 书

Product Specification

Model Name (产品名称)	TFT-LCD Module
Part Number (产品型号)	JT366FHI51RSL01

Item (项目)	Prepared (拟制)	Checked (审核)	Approved (批准)
Signature (签名)			
Date (日期)			
Note (备注)			

Customer: (客户)

Signature (签名)	
Date (日期)	

Revision Record

Version	Issued Date	Page	Old Description	New Description
01	2021-05-11	\	Initial release	\
		\		

CONTENTS

1. General Description

This specification applies to the 36.6 inch Color TFT-LCD SKD model. This open cell unit has a TFT active matrix type liquid crystal panel 1920x290 pixels, and diagonal size of 36.6 inch. This module supports 1920x290 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot.

It has been designed to apply the 8 lane LVDS interface method. It is intended to support displays where high brightness, wide viewing angle, high color saturation, and high color depth are very important.

*** General Information**

Items	Specification	Unit	Note
Active Screen Size	36.6	inch	
Display area	919.3(H)*138.85(V)	mm	
Driver Element	a-Si TFT active matrix		Driver Element
Bezel width (L/R/U/D)	16.8/16.8/16.75/16.75	mm	
Overall dimensions	960(H)*174.35(V)16.9(D)	mm	
Display Colors	8 bit, 16.7M	Colors	
Frame rate	60	Hz	See Chapter 5.1 for details
Number of Pixels	1920x290	Pixel	
Pixel Pitch	0.4788 (H) x 0.4788 (W)	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Surface Treatment	Anti-Glare, 3H		Haze=2%
Transmittance (with Polarizer)	5.5 %		Typical value, Note 1
Weight	Typ TBD	g	
Display Orientation	Signal input with “ABC”		Note 2

Note 1: Light source here is the BLU of AUO module (film structure: two diffuser sheets).

Note 2: LCD display as below illustrated when signal input with “ABC”.

2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit or the unrecoverable damage on the device.

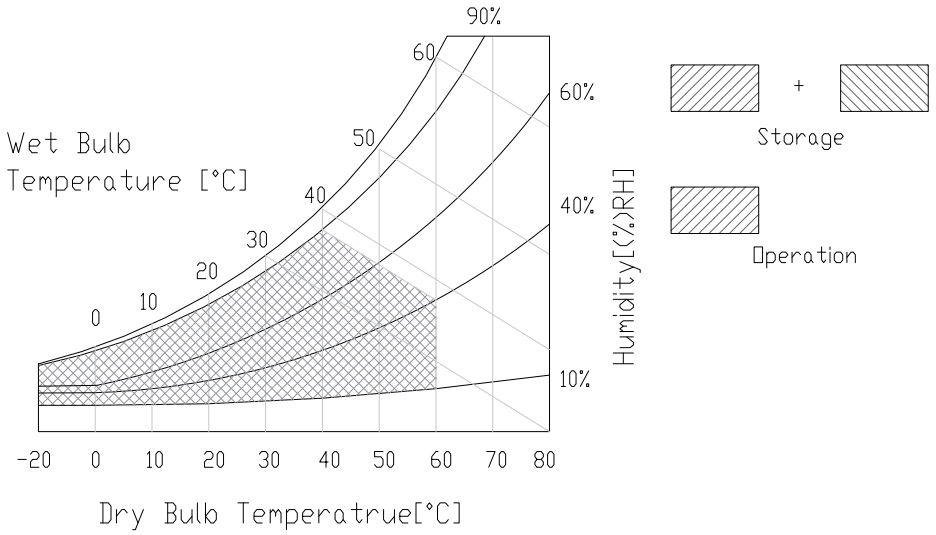
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V_{DD}	-0.3	14	[Volt] $_{DC}$	Note 1
Input Voltage of Signal	Vin	-0.3	4	[Volt]$_{DC}$	Note 1
Operating Temperature	TOP	-20	+60	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	Note 3

Note 1: Duration:50 msec.

Note 2 : Maximum Wet-Bulb should be 39℃ and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃.

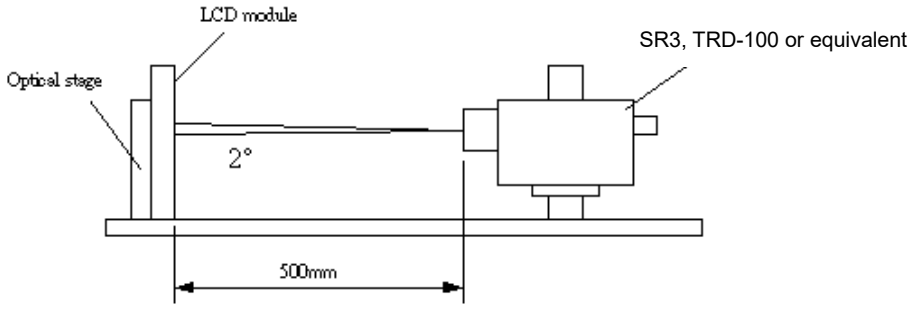
Note 3: Surface temperature is measured at 50℃ Dry condition



3. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25°C. The values specified are measured on the center of active area and at an approximate distance 500 mm from the LCD surface at a viewing angle of φ and θ equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



Parameter	Symbol	Condition	Values			Unit	Notes
			Min.	Typ.	Max		
Contrast Ratio	CR	SR3, TRD-100	3200	4000	--		1, 2
Response Time (G to G)	T_{γ}		--	8	16	ms	3
Gamma	Gma		1.9	2.2	2.5		6
Color Chromaticity		With SR3 Standard light source "C"					4
Red	R_X		Typ.-0.03	0.662	Typ.+0.03		
	R_Y			0.325			
Green	G_X			0.276			
	G_Y			0.591			
Blue	B_X			0.136			
	B_Y			0.109			
White	W_X			0.2953			
	W_Y			0.348			
Viewing Angle		With AUO Module					1, 5
x axis, right(φ=0°)	θ_r		85	89	--	degree	
x axis, left(φ=180°)	θ_l		85	89	--	degree	
y axis, up(φ=90°)	θ_u		85	89	--	degree	
y axis, down (φ=270°)	θ_d		85	89	--	degree	
Brightness			900	1000	--	cd/m^2	

1. Light source here is the BLU of AUO module (film structure: two diffuser sheets).
2. Contrast Ratio (CR) is defined mathematically as:

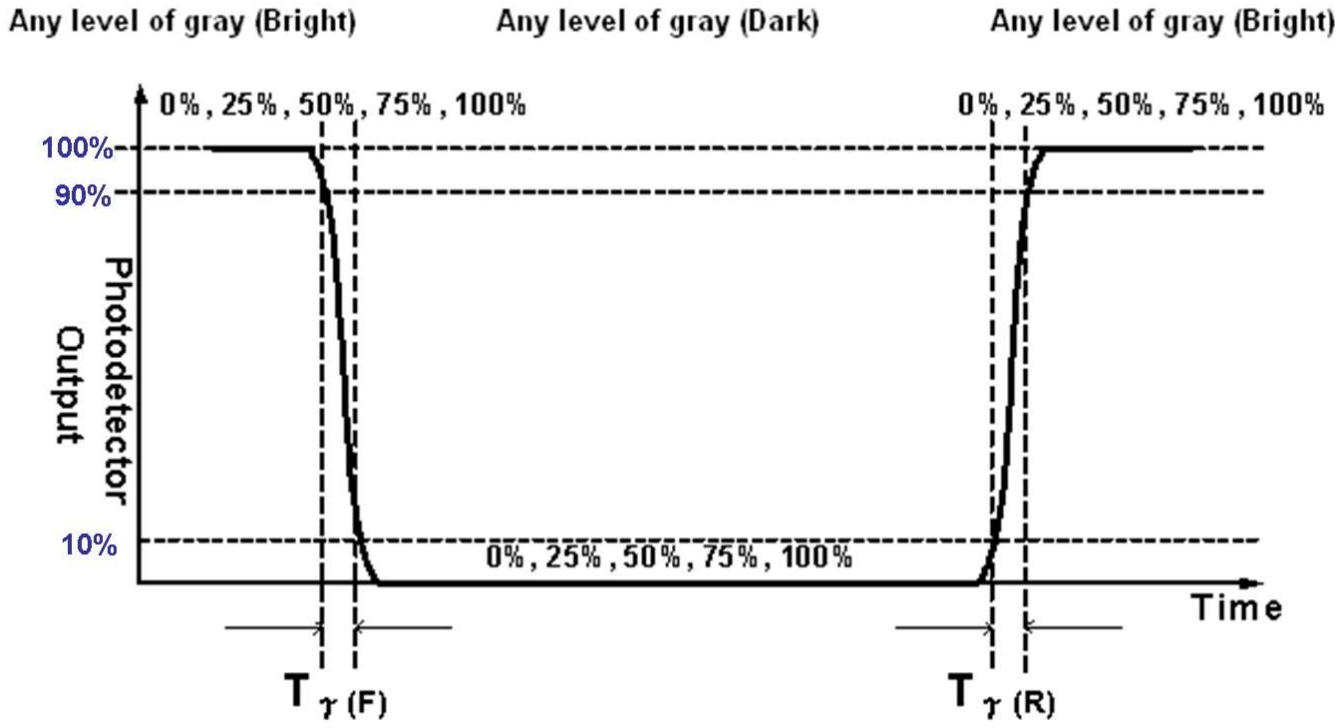
$$\textbf{Contrast Ratio} = \frac{\textbf{Surface Luminance at center location of all white pixels}}{\textbf{Surface Luminance at center location of all black pixels}}$$

3. Response time T_γ is the average time required for display transition by switching the input signal for five luminance ratio (0%,25%,50%,75%,100% brightness matrix) and is based on Frame rate =60Hz to optimize.

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

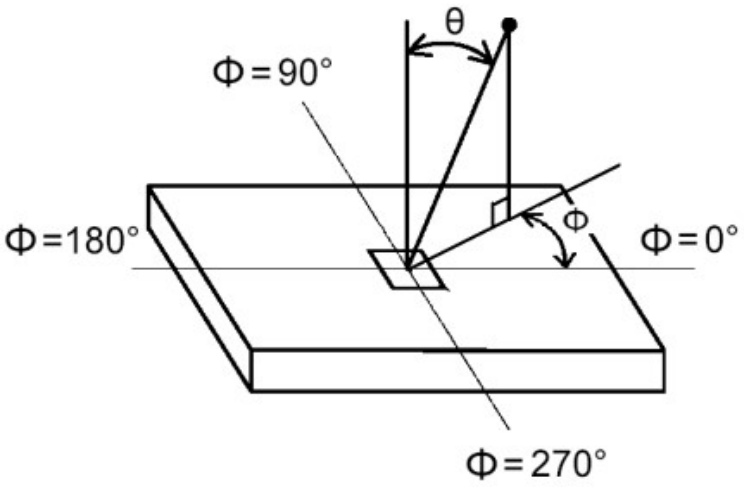
T_γ is determined by 10% to 90% brightness difference of rising or falling period. (As illustrated)
The response time is defined as the following figure and shall be measured by switching the input signal for "any level of gray(bright) " and "any level of gray(dark)".

FIG.3 Response Time



4. Light source here is the standard light source "C" which is defined by CIE and driving voltages are based on suitable gamma voltages. The calculating method is as following :
   A. Measure the "Module" and "BLU" optical spectrums (W, R, G, B).
   B. Calculate cell spectrum from "Module" and "BLU" spectrums.
   C. Calculate color chromaticity by using cell spectrum and the spectrum of standard light source "C".
5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG4.

FIG.4 Viewing Angle



6. Gamma value is measured between L25 to L128.

4. Interface Specification

4.1 Input power

The P366IVN01.0 Open Cell Unit requires power input which is employed to power the LCD electronics and to drive the TFT array and liquid crystal.

Item		Symbol	Min.	Typ.	Max	Unit	Note
Power Supply Input Voltage		V_{DD}	10.8	12	13.2	V	1
Power Supply Input Current	Black pattern	I_{DD}	-	0.2	0.24	A	2
	White pattern		-	0.2	0.24	A	
	H-strip pattern		-	0.3	0.36	A	
Power Consumption	Black pattern	P_C	-	2.4	2.88	Watt	
	White pattern		-	2.4	2.88	Watt	
	H-strip pattern		-	3.6	4.32	Watt	
Inrush Current		I_{RUSH}	--	--	2	A	3

Note1. The ripple voltage should be fewer than 5% of VDD.

Note2. Test Condition:

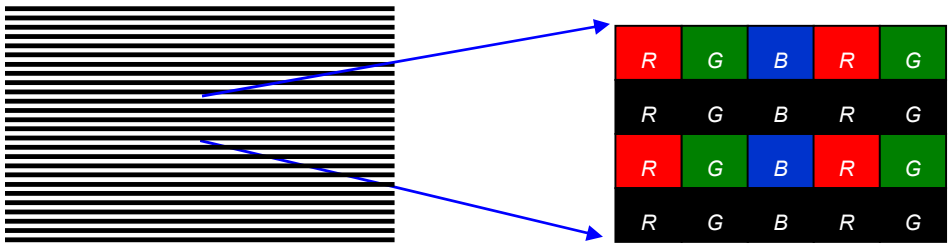
(1) V_{DD} = 12V, (2) Fv = 60Hz, (3) Fclk= 74.25MHz, (4) Temperature = 25 ℃

(5) Power dissipation check pattern. (Only for power design)

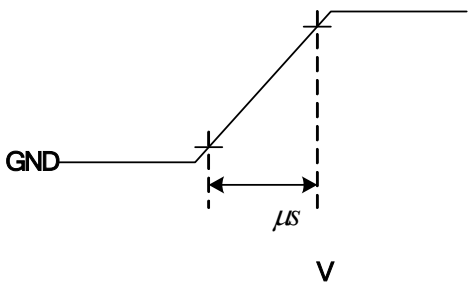
a. Black pattern

b. White pattern

c. H-Strip pattern



Note3. Measurement condition : Rising time = 400us

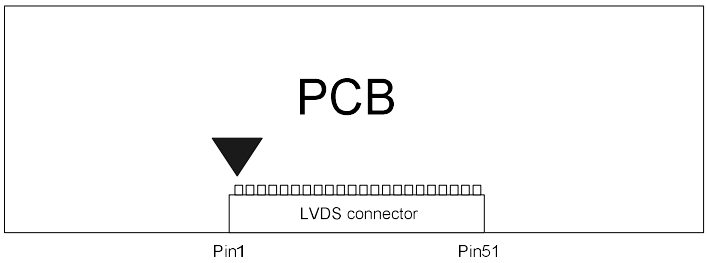


4.2 Input Connection

■ LCD connector: JAE SJ11346-FI-RTE51SZ-HF / P-Two 187059-5122 / Starconn 115E51-0000RA-M3-R

PIN	Symbol	Description	Note	PIN	Symbol	Description	Note
1	N.C.	No connection	2	26	N.C.	No connection	2
2	SCL	I2C Clock	4	27	N.C.	No connection	2
3	WP	Write Protection	5	28	CH2_Y0-	LVDS Channel 2, Signal 0-	
4	SDA	I2C Data	4	29	CH2_Y0+	LVDS Channel 2, Signal 0+	
5	N.C.	No connection	2	30	CH2_Y1-	LVDS Channel 2, Signal 1-	
6	N.C.	No connection	2	31	CH2_Y1+	LVDS Channel 2, Signal 1+	
7	LVDS_SEL	Open/High(3.3V) for NS, Low(GND) for JEIDA	6	32	CH2_Y2-	LVDS Channel 2, Signal 2-	
8	N.C.	No connection	2	33	CH2_Y2+	LVDS Channel 2, Signal 2+	
9	N.C.	No connection	2	34	GND	Ground	
10	N.C.	No connection	2	35	CH2_CLK-	LVDS Channel 2, Clock -	
11	GND	Ground		36	CH2_CLK+	LVDS Channel 2, Clock +	
12	CH1_Y0-	LVDS Channel 1, Signal 0-		37	GND	Ground	
13	CH1_Y0+	LVDS Channel 1, Signal 0+		38	CH2_Y3-	LVDS Channel 2, Signal 3-	
14	CH1_Y1-	LVDS Channel 1, Signal 1-		39	CH2_Y3+	LVDS Channel 2, Signal 3+	
15	CH1_Y1+	LVDS Channel 1, Signal 1+		40	N.C.	No connection	2
16	CH1_Y2-	LVDS Channel 1, Signal 2-		41	N.C.	No connection	2
17	CH1_Y2+	LVDS Channel 1, Signal 2+		42	N.C.	No connection	2
18	GND	Ground		43	N.C.	No connection	2
19	CH1_CLK-	LVDS Channel 1, Clock -		44	GND	Ground	
20	CH1_CLK+	LVDS Channel 1, Clock +		45	GND	Ground	
21	GND	Ground		46	GND	Ground	
22	CH1_Y3-	LVDS Channel 1, Signal 3-		47	N.C.	No connection	2
23	CH1_Y3+	LVDS Channel 1, Signal 3+		48	V_{DD}	Power Supply, +12V DC Regulated	
24	N.C.	No connection	2	49	V_{DD}	Power Supply, +12V DC Regulated	
25	N.C.	No connection	2	50	V_{DD}	Power Supply, +12V DC Regulated	
				51	V_{DD}	Power Supply, +12V DC Regulated	

Note1. Pin number start from the left side as the following figure.



Note2. Please leave this pin unoccupied. It can not be connected by any signal (Low/GND/High).

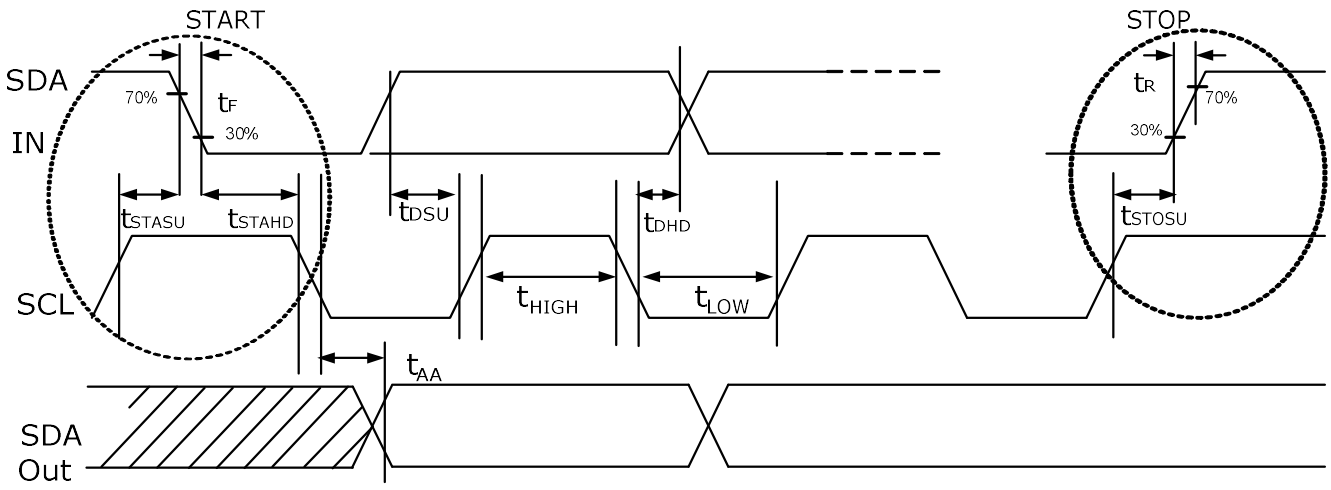
Note3. Input control signal threshold voltage definition

Item	Symbol	Min.	Typ.	Max.	Unit
Input High Threshold Voltage	VIH	2.7	-	3.6	V
Input Low Threshold Voltage	VIL	0	-	0.6	V

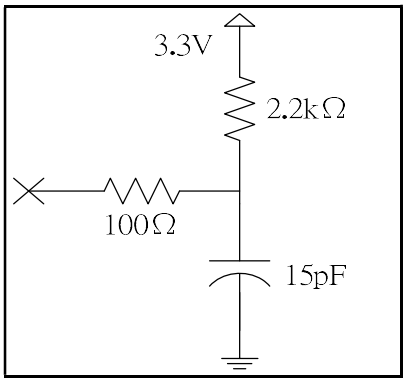
Note4. I2C Data and Clock

I2C Data and Clock timing

Parameter		Symbol	Min.	Typ.	Max	Unit
I2C	SCL clock frequency	fSCL	-	-	350	kHz
	Clock Pulse Width Low	tLOW	1.85	-	-	us
	Clock Pulse Width High	tHIGH	0.4	-	-	us
	Clock Low to Data Output Valid	tAA	1.76	-	-	us
	Start Setup Time	tSTASU	0.6	-	-	us
	Start Hold Time	tSTAHD	0.6	-	-	us
	Stop Setup Time	tSTOSU	0.6	-	-	us
	Data In Setup Time	tDSU	0.1	-	-	us
	Data In Hold Time	tDHD	0	-	-	us
	SCL/SDA Rise Time	tR	-	-	0.3	us
	SCL/SDA Fall Time	tF	-	-	0.3	us



Input equivalent impedance of SDA/SCL pin

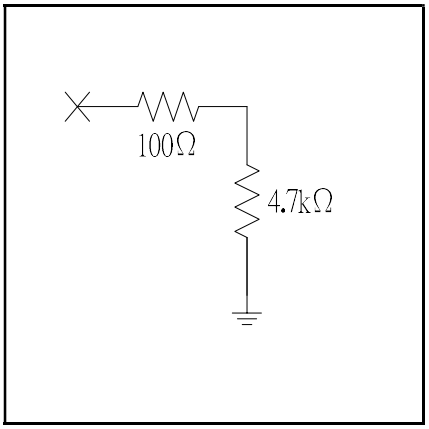


Note5. Write Protection

Mode selection

WP	Note
L or OPEN	Protection
H	Writable

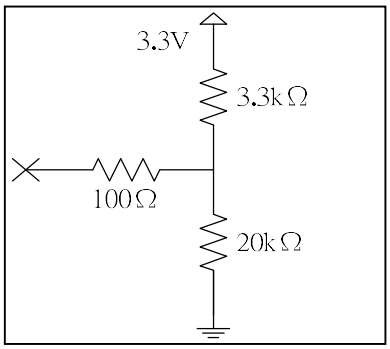
Input equivalent impedance of WP pin



Note6. LVDS data format selection

LVDS_SEL	Mode
H	NS
L or OPEN	Jeida

Input equivalent impedance of LVDE_SEL pin



4.3 Input Data Format

4.3.1 V by one color data mapping

Mode		Packer input & Unpacker output		30bpp RGB /YCbCr444 (10bit)	24bpp RGB /YCbCr444 (8bit)
4byte mode	3byte mode	Byte0	D[0]	R/Cr[2]	R/Cr[0]
			D[1]	R/Cr[3]	R/Cr[1]
			D[2]	R/Cr[4]	R/Cr[2]
			D[3]	R/Cr[5]	R/Cr[3]
			D[4]	R/Cr[6]	R/Cr[4]
			D[5]	R/Cr[7]	R/Cr[5]
			D[6]	R/Cr[8]	R/Cr[6]
			D[7]	R/Cr[9]	R/Cr[7]
		Byte1	D[8]	G/Y[2]	G/Y[0]
			D[9]	G/Y[3]	G/Y[1]
			D[10]	G/Y[4]	G/Y[2]
			D[11]	G/Y[5]	G/Y[3]
			D[12]	G/Y[6]	G/Y[4]
			D[13]	G/Y[7]	G/Y[5]
			D[14]	G/Y[8]	G/Y[6]
			D[15]	G/Y[9]	G/Y[7]
		Byte2	D[16]	B/Cb[2]	B/Cb[0]
			D[17]	B/Cb[3]	B/Cb[1]
			D[18]	B/Cb[4]	B/Cb[2]
			D[19]	B/Cb[5]	B/Cb[3]
			D[20]	B/Cb[6]	B/Cb[4]
			D[21]	B/Cb[7]	B/Cb[5]
			D[22]	B/Cb[8]	B/Cb[6]
			D[23]	B/Cb[9]	B/Cb[7]
		Byte3	D[24]	--	
			D[25]	--	
			D[26]	B/Cb[0]	
			D[27]	B/Cb[1]	
			D[28]	G/Y[0]	
			D[29]	G/Y[1]	
			D[30]	R/Cr[0]	
			D[31]	R/Cr[1]	

4.3.2 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 8 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

Color		Input Color Data																							
		RED								GREEN								BLUE							
		MSB							LSB	MSB							LSB	MSB							LSB
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

4.4 Backlight Specification

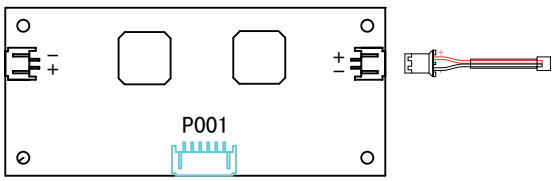
Electrical specification

Parameter			Symbol	Values			Unit	notes
				Min	Typ	Max		
LED Driver :								
Power Supply Input Voltage			VBL	10.8	12.0	13.2	Vdc	1
Power Supply Input Current			IBL	-	2.66	2.72	A	1
Power Supply Input Current (In-Rush)			In-rush	-	-	(TBD)	A	V_{BL} = 12.0V $ExtV_{BR-B}$ = 100% 3
Power Consumption			PBL	-	32	36	W	1
Input Voltage for Control System Signals	On/Off	On	V on	2.5	-	5.5	Vdc	
		Off	V off	-0.3	0.0	0.5	Vdc	
	Brightness Adjust		$ExtV_{BR-B}$	30	-	100	%	On Duty 5
				30	-	100	%	
	$ExtV_{BR-B}$ Frequency		f_{PWM}	500	-	1500	Hz	
	Pulse Duty Level (PWM)		High Level	2.5	-	5.5	Vdc	HIGH : on duty LOW : off duty
			Low Level	0.0	-	0.5	Vdc	
LED :								
Life Time				30,000	50,000		Hrs	2

notes :

1. Electrical characteristics are determined after the unit has been 'ON' and stable for approximately 60 minutes at 25±2°C. The specified current and power consumption are under the typical supply Input voltage 24Vand V_{BR} ($ExtV_{BR-B}$: 100%), it is total power consumption.
2. The life time (MTTF) is determined as the time which luminance of the LED is 50% compared to that of initial value at the typical LED current (ExtVBR-B :100%) on condition of continuous operating in LCM state at 25±2°C.
3. The duration of rush current is about 200ms. This duration is applied to LED on time.
4. Even though inrush current is over the specified value, there is no problem if I^2T spec of fuse is satisfied. $ExtV_{BR-B}$ signal have to input available duty range and sequence.
5. After Driver ON signal is applied, $ExtV_{BR-B}$ should be sustained from 30% to 100% more than 500ms. After that, $ExtV_{BR-B}$ 30% and 100% is possible

4.4.1 LIGHTBAR Connector Pin Assignment



LED驱动板

P001:Input terminal **PH2.0-6 (2.0mm X 6)**

Pin No.	Symbol	Description	note
1	VCC	Power supply voltage +12V	
2	VCC	Power supply voltage +12V	
3	ON/OFF	Output enable signal	
4	DIM	Dimming signal	
5	GND	Power ground	
6	GND	Power ground	

5. Signal Timing Specification

5.1 Input Timing

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

5.1.1 Timing Table (DE only Mode)

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	1120	1120	1120	Th
	Active	Tdisp (v)	1080			
	Blanking	Tblk (v)	40	40	40	Th
Horizontal Section	Period	Th	1060	1060	1060	Tclk
	Active	Tdisp (h)	960			
	Blanking	Tblk (h)	100	100	100	Tclk
Clock	Frequency	Fclk=1/Tclk	53	74.25	82	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	60	67.5	73	KHz

Notes:

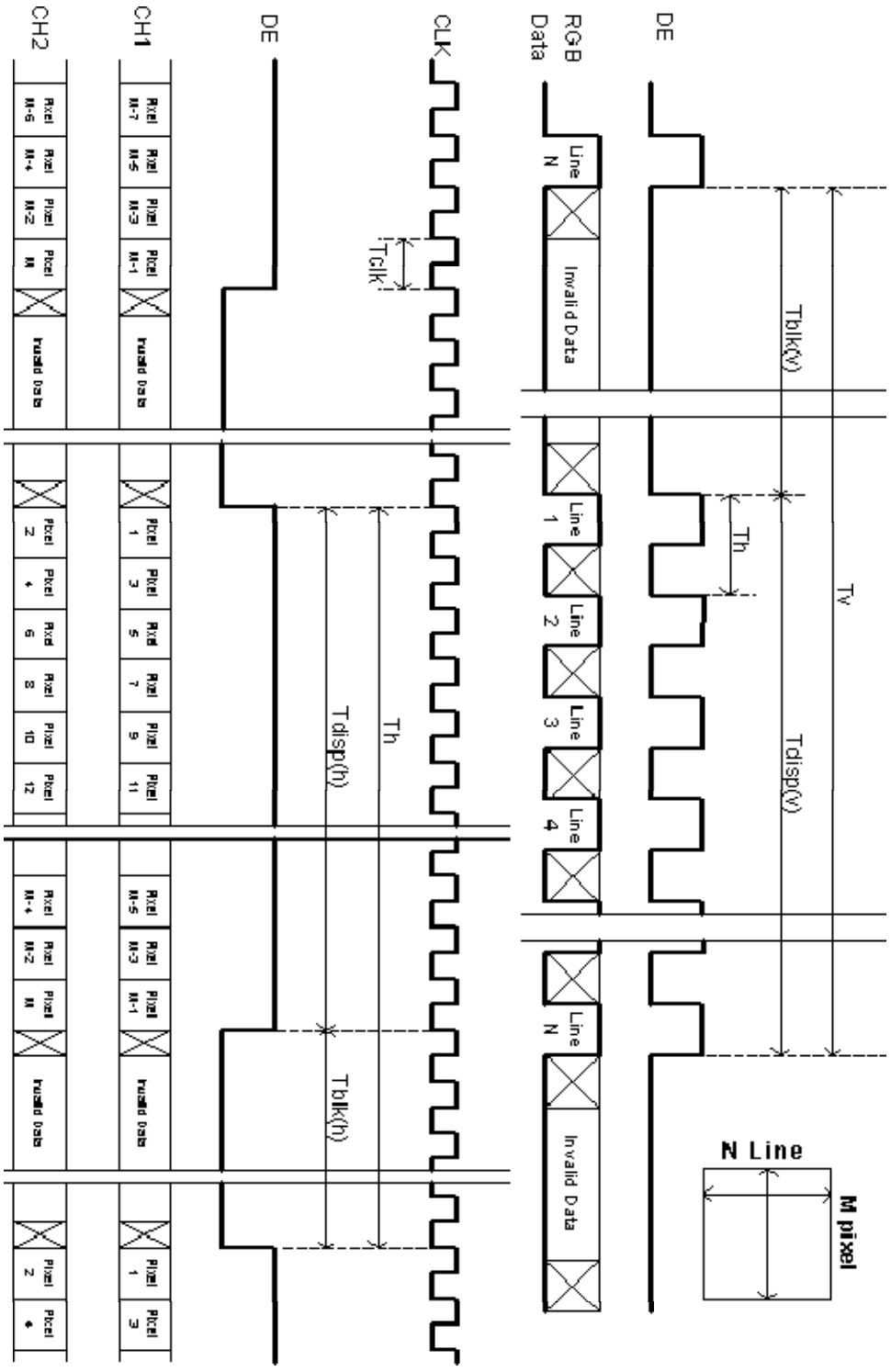
(1) Display position is specific by the rise of DE signal only.
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.

(2)Vertical display position is specified by the rise of DE after a “Low” level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.

(3)If a period of DE “High” is less than 3840 DCLK or less than 2160 lines, the rest of the screen displays black.

(4)The display position does not fit to the screen if a period of DE “High” and the effective data period do not synchronize with each other.

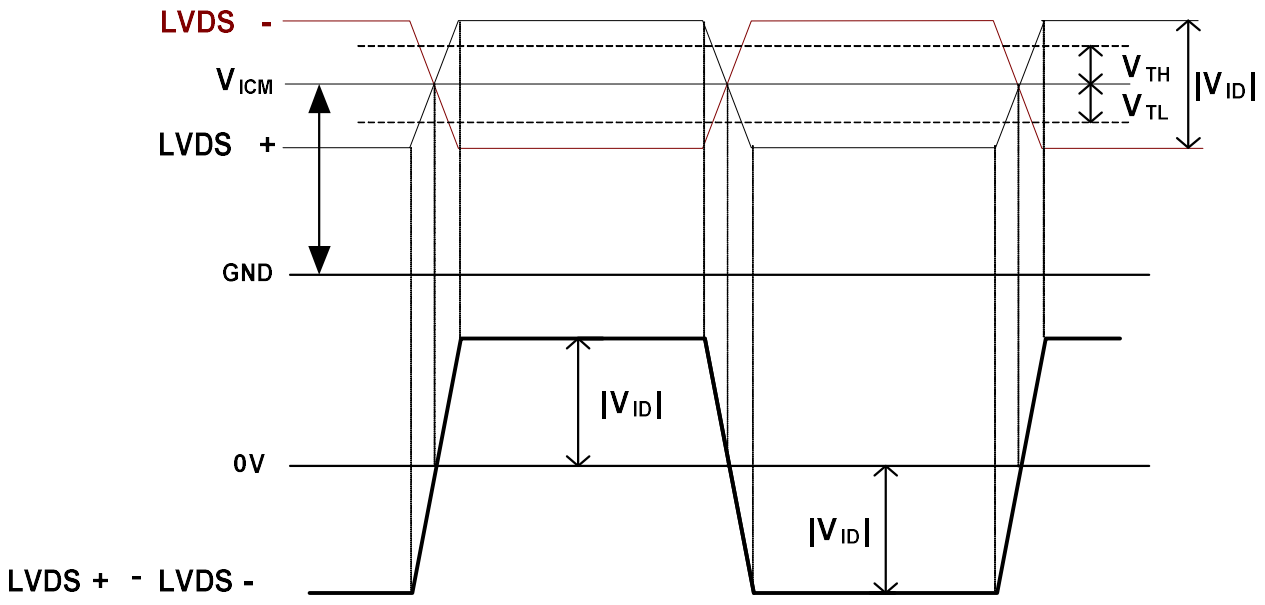
5.1.2 The timing diagrams of the input timing



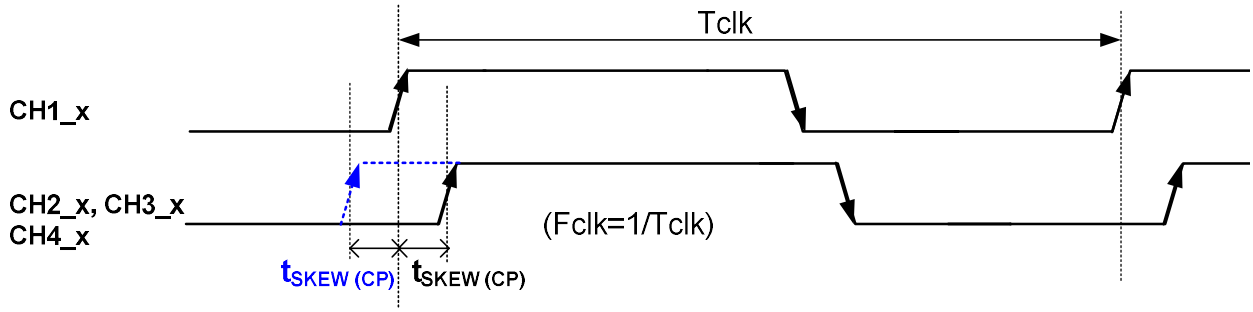
5.2 Input interface characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LVDS Interface	Input Differential Voltage	$\lvert V_{ID} \rvert$	100	400	600	mV_{DC}	1
	Differential Input High Threshold Voltage	V_{TH}	--	--	+100	mV_{DC}	1
	Differential Input Low Threshold Voltage	V_{TL}	-100	--	--	mV_{DC}	1
	Input Common Mode Voltage	V_{ICM}	1.1	1.25	1.4	V_{DC}	1
	Input Channel Pair Skew Margin	$t_{SKEW\ (CP)}$	-500	--	+500	ps	2
	Input Channel Pair Skew Margin (only for M'Star MST7428BB)	$t_{SKEW\ (CP)}$	-400	--	+400	ps	2
	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	--	Fclk +3%	MHz	3
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30	--	200	KHz	3
	Receiver Data Input Margin Fclk = 85 MHz Fclk = 65 MHz	tRMG	 -0.4 -0.5	 -- --	 0.4 0.5	ns	8

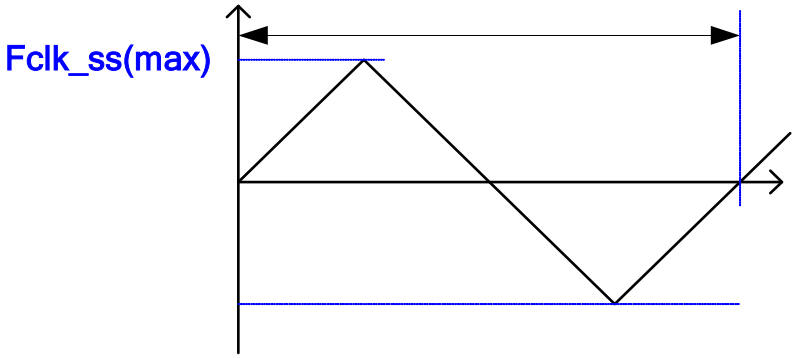
Note1. VICM = 1.25V



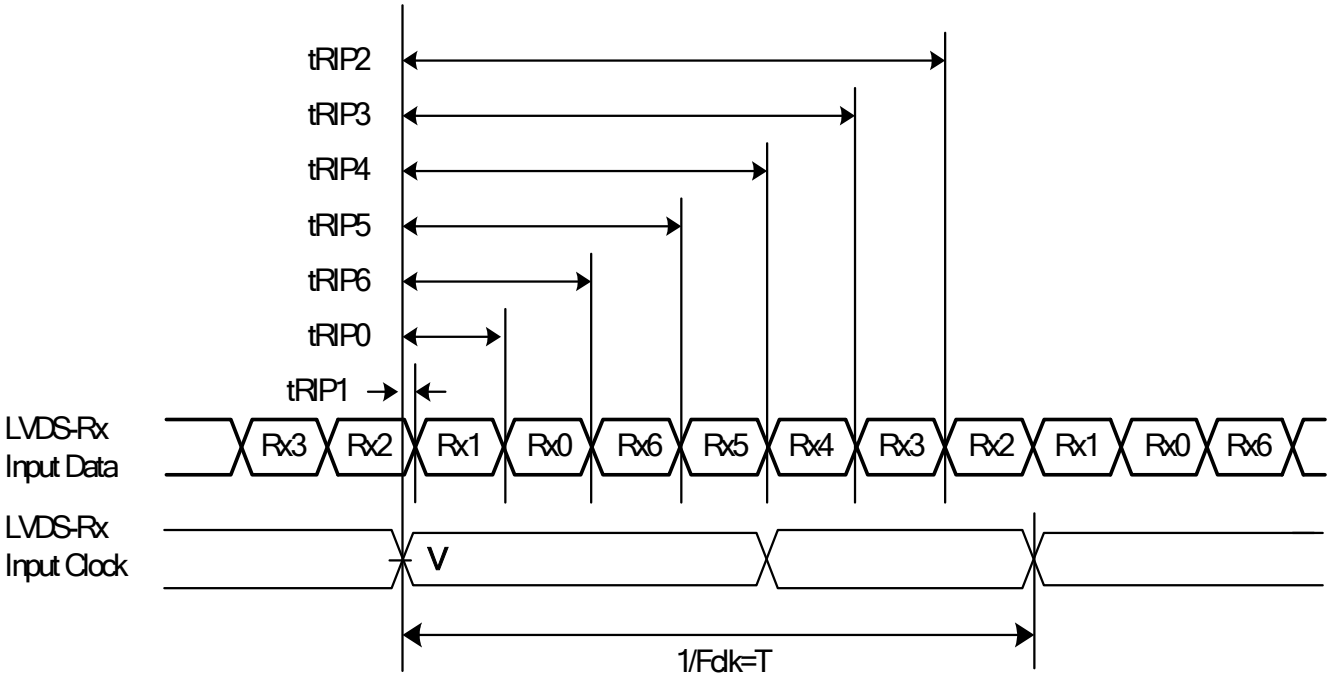
Note2. Input Channel Pair Skew Margin



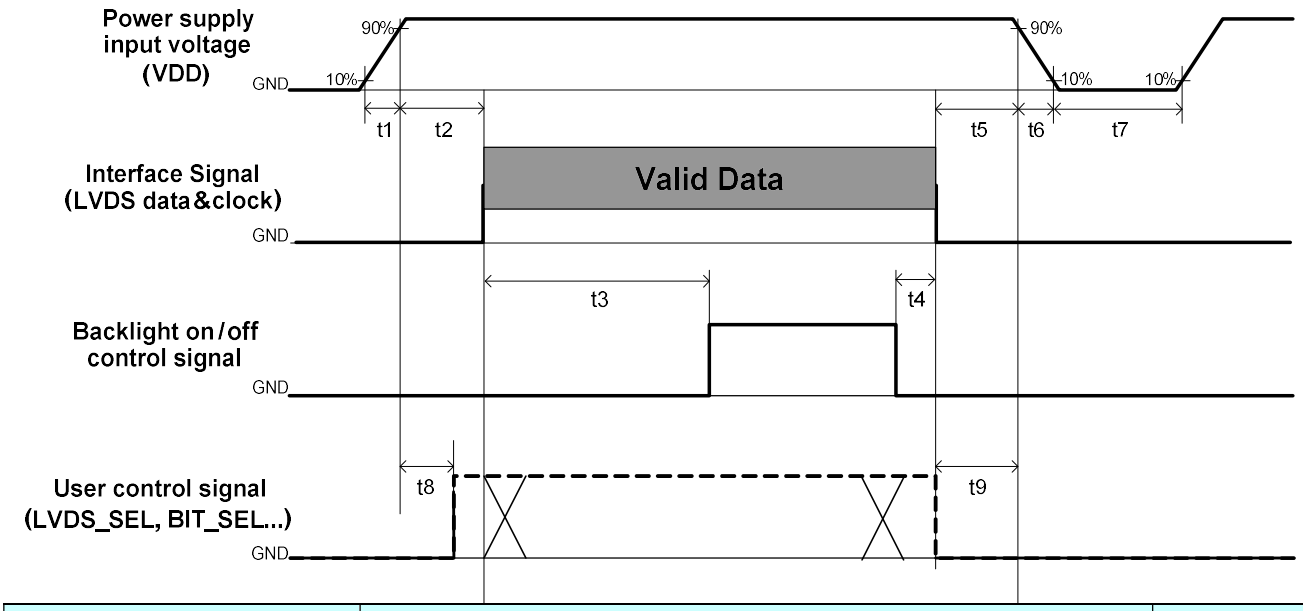
Note3. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures.



		Min	Type	Max		
Input Clock Frequency	Fclk	Fclk (min)	--	Fclk (max)	MHz	**T=1/Fclk**
Input Data Position0	tRIP1	-|tRMG|	0	|tRMG|	ns	
Input Data Position1	tRIP0	T/7-|tRMG|	T/7	T/7+|tRMG|	ns	
Input Data Position2	tRIP6	2T/7-|tRMG|	2T/7	2T/7+|tRMG|	ns	
Input Data Position3	tRIP5	3T/7-|tRMG|	3T/7	3T/7+|tRMG|	ns	
Input Data Position4	tRIP4	4T/7-|tRMG|	4T/7	4T/7+|tRMG|	ns	
Input Data Position5	tRIP3	5T/7-|tRMG|	5T/7	5T/7+|tRMG|	ns	
Input Data Position6	tRIP2	6T/7-|tRMG|	6T/7	6T/7+|tRMG|	ns	



5.3 Power Sequence for LCD



Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2	0.1	---	50	ms
t3	400	---	---	ms
t4	0 *1	---	---	ms
t5	0	---	---	ms
t6	---	---	--- *2	ms
t7	1000 *3	---	---	ms
t8	20 *4	---	50	ms
t9	0	---	---	ms

Note:

(1) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)

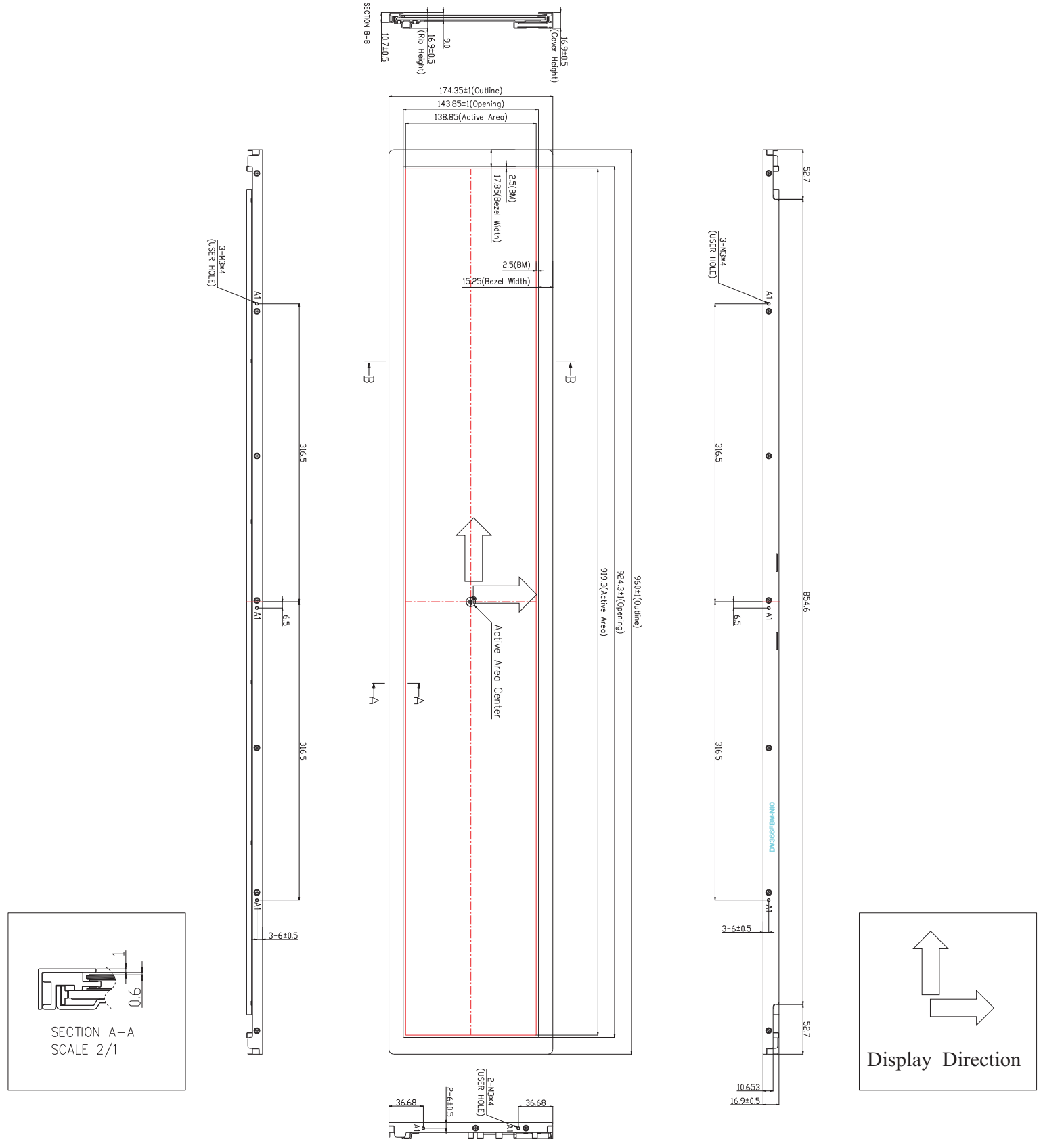
(2) When CMOS Interface signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.

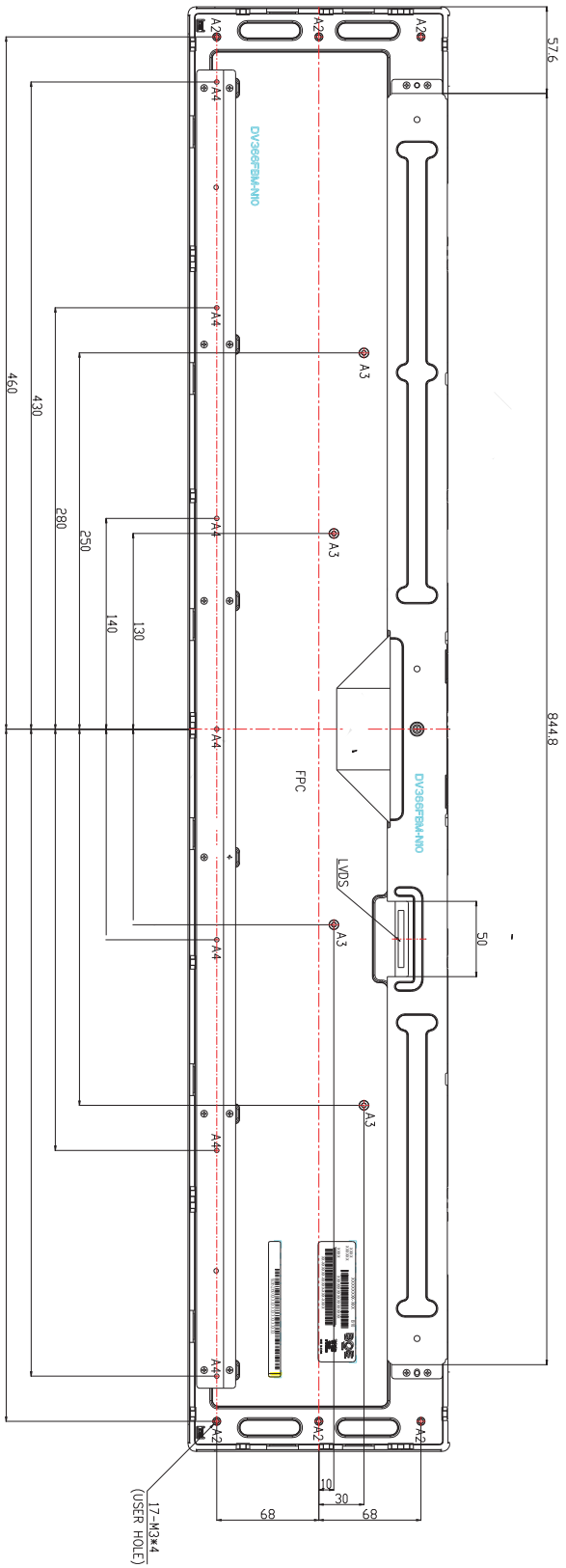
6. Mechanical Characteristics

Table 10. MECHANICAL CHARACTERISTICS

Item	Value	
Outline Dimension	Horizontal	960mm
	Vertical	174.35mm
	Thickness	16.9mm
Active Display Area	Horizontal	919.3mm
	Vertical	138.85mm
Weight	TBDkg (Typ.)	
umber of Pixels	1920x290 Pixel	

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.


SECTION B-B
10.7±0.5
16.9±0.5 (Rib Height)
9.0
16.9±0.5 (Cover Height)
174.35±1(Outline)
143.85±1(Opening)
138.85(Active Area)
2.5(BM)
17.85(Bezel Width)
2.5(BM)
15.25(Bezel Width)
3-M3*4 (USER HOLE)
316.5
6.5
3-6±0.5
960±1(Outline)
924.3±1(Opening)
919.3(Active Area)
Active Area Center
52.7
854.6
10.653
16.9±0.5
2-M3*4 (USER HOLE)
2-6±0.5
36.68
SECTION A-A
SCALE 2/1
Display Direction



ITEM NO.	DESCRIPTION	TYPE	UDM Height (mm)	Max. Depth (mm)	Torque kgf·cm
A1	M3	Short Rivet	0.0	4.0	Max.5.0
A2	M3	Middle Rivet	6.0	5.0	Max.5.0
A3	M3	Longt Rivet	7.7	5.0	Max.5.0
A4	M3	Thread Hole	0.0	5.0	Max.5.0

7. Packing

TBD

8. Precautions

Please pay attention to the followings when you use this TFT LCD Open Cell unit and strongly recommended to contact AUO if module process advice is required.

8.1 Storage

When storing open cell units, the following precautions are necessary.

(a) Store them in a dark place. Do not expose the open cell unit to sunlight or fluorescent light.

(b) Store them at the advised storage temperature between 5℃ and 35℃ at normal humidity (35%rH~75%rH).

(c) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

(d) Be careful of condensation. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

8.2 Module Assembly

8.2.1 Protection film peeling

(a) The protection films of polarizer had attached on the both sides of open cell polarizer surfaces. Handlers should peel them off with care. While the protection film is being peeled off, static electricity is easily generated on the polarizer surface. Please follow the instructions listed below to reduce ESD failure risk.

(b) People who handle the unit should wear antistatic wristbands on hands. The band should be connected to the common ground with a current limiting resistor which is most commonly one megohm, rated at least 1/4 watt with a working voltage rating of 250 volts.

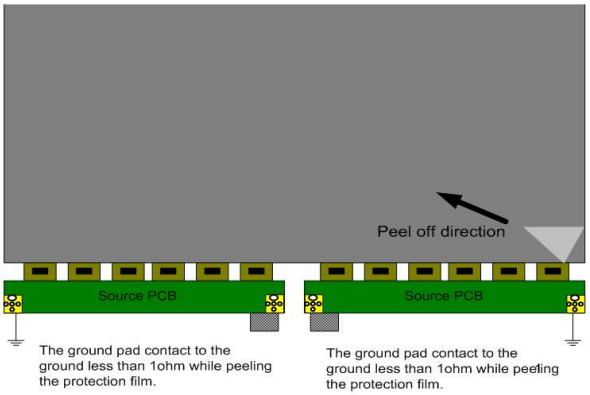
(c) Connect the grounded pads on source PCB to ground with less than 1 ohm resistance as below figure.

(d) The peeling direction is recommended in below figure.

(e) During peeling off process, ionized air should continuously & stably be blown on the surfaces of protection film and polarizer. The flow rate of ionized air should be monitored periodically.

(f) It is recommended to peel protection films off as slowly as possible. (constant speed more than 8 seconds per film.)

(g) The protection film should not be contacted to the IC (source and gate) or source PCB.



8.2.2 Assembly Precautions

(a) Remove the stains with finger-stalls wearing soft gloves in order to keep the display clean in the process of the incoming inspection and the assembly process. When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.

(b) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer with bare hands or greasy clothes. (Some cosmetics are detrimental to the polarizer.)

(c) Use the tray to transport open cell can prevent open cell broken and electrical components damage.

(d) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the cell. And the frame on which a cell is mounted should have sufficient strength so that external force is not transmitted directly to the cell

(e) Be careful not to give any extra mechanical stress to the panel when designing the set, and BLU kit.

(f) Do not use cover case which made of acetic acid type and chlorine type materials because acetic acid type materials generates corrosive gas which will damage the polarizer at high temperature and chlorine type materials causes circuit break by electro-chemical reaction.

(g) When the panel kit and BLU kit are assembled, the panel kit and BLU kit should be attached to the set system firmly by combining each mounted holes. Be careful not to give the mechanical stress. Electrostatic discharge may easily damage the electronic circuits on the open cell unit. Make certain that treatment persons are grounded, (ex: anti-static wristband or etc) and don’t touch interface pin directly.

8.2.3 FFC & PCB Precautions

(a) Refrain from applying any forces to the source PCB and the drive IC in the process of the handling or installing to the set. If any forces are applied to the product, it may cause damage or a malfunction in the panel kit.

(b) Do not pull, fold or bend the source COF and the gate COF in any processes.

(c) This panel has its circuitry of PCB's on the rear side, so it should be handled carefully in order for a force not to be applied.

(d) Do not touch the pins of the interface connector directly with bare hands.

(e) The connector is a precision device to connect PCB and transmit electrical signals. Operators should plug/un-plug the connector in parallel way during module assembly.

(f) The cables between TV SET connector and Control PCB interface should be connected directly to have a minimized length. A longer cable between TV SET connector and Control PCB interface maybe operate abnormal display.

8.2.4 Flicker adjust

In order to prevent potential problems, flicker should be adjusted by optimizing the Vcom value in customer LCM Line through the I2C Interface. Detail settings please refer to appendix section.

8.3 Aging

Be sure to age for over 1 hour at least, which the product is driving initially to stabilize TFT Characteristic.

8.4 Operating Precautions

(a) Be cautious not to give any strong mechanical shock or any forces to the panel kit. Applying any forces to the panel may cause the abnormal operation or the damage to the panel kit and the back light unit kit.

(b) Avoid the condensation of water which may result in the improper operation of product.

(c) It is recommended to operate the LCD product under normal operating conditions as below

- VDD=12V
- Temperature=25±10℃
- Display pattern: continually changing pattern

(d) Response time depends on the temperature. (In lower temperature, it becomes longer)

(e) If the product will be used under extreme conditions such as under high temperature, humidity, display patterns or the operation time etc.., it is strongly recommended to contact AUO for the advice about the application of engineering. Otherwise, its reliability and the function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock markets, and controlling systems.

(f) Operation usage to protect against image sticking due to long-term static display.

A. Suitable operating time: 24 hours a day or less.
B. Liquid Crystal refresh time is required. Cycling display between 5 minutes' information (static) display and 10 seconds' moving image.
C. Periodically change background and character (image) color.
D. Avoid combination of background and character with large different luminance.

(g)Periodically adopt one of the following actions after long time display.

A. Running the screen saver (motion picture or black pattern)
B. Power off the system for a while

(h)Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions, such as high temperature/ humidity, display stationary patterns, or long operation time etc…, it is strongly recommended to contact AUO for filed application engineering advice. Otherwise, its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock market and controlling systems.

8.5 Others

(a) Module designer should apply adequate thermal solutions to keep the electrical components surface temperature under control limit (ex: Source Driver IC 100℃, Components on T-con PCB 85℃) Operations over the temperature can cause damages or decrease of lifetime.

(b) Protect the TFT LCD open cell unit out of the static electricity in all process. Otherwise the circuit IC could be damaged.

Reference: The environment ESD control standard of AUO

Item	Control standard
ESD	All environment ESD controlled under 200V
Ground resistance	All equipment ground should be less than 1ohm.

(c) Note that polarizer could be damaged easily. Do not press or scratch the bare surface with the material which is harder than a HB pencil lead.

(d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time on the product, the stain or the discoloration may occur.

(e) If the surface of the polarizer is dirty, clean it using the absorbent cotton or the soft cloth.

(f) If the liquid crystal material leaks from the panel, this should be kept away from the eyes or mouth. If this contacts to hands, legs, or clothes, you must washed it away with soap thoroughly and see a doctor for the medical examination.

(g) The module has high frequency circuits. The sufficient suppression to the electromagnetic interference should be done by the system manufacturers. The grounding and shielding methods is important to minimize the interference. The sufficient suppression to the EMI should be done by the set manufacturers.