产 品 规 格 书

Product Specification

Model Name (产品名称)	TFT-LCD Module
Part Number (产品型号)	JT364FHI51R5L01

Item (项目)	Prepared (拟制)	Checked (审核)	Approved (批准)
Signature (签名)	赖依	林勇	
Date (日期)	2022-04-12	2022-04-12	
Note (备注)			

Customer: (客户)

Signature (签名)	
Date (日期)	

Revision Record

Version	Issued Date	Page	Old Description	New Description
01	2022-04-12	\	Initial release	\

CONTENTS

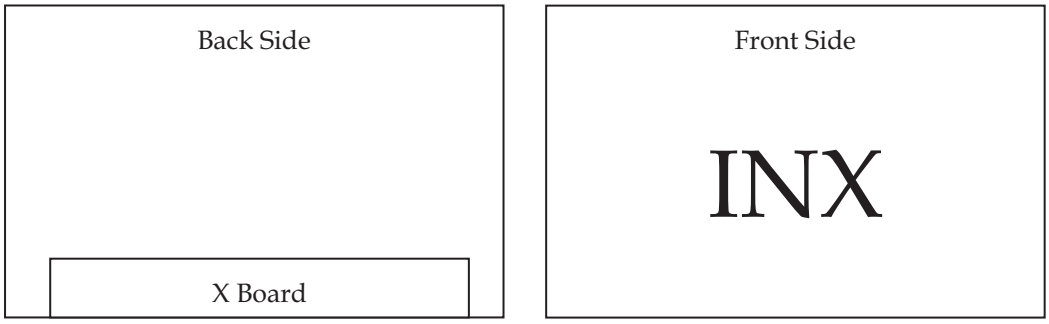
1. GENERAL DESCRIPTION

1.1 OVERVIEW

This is a 36.4″ TFT Liquid Crystal Display TV product with driver ICs and 2ch-LVDS interface. This product supports 1920 x 641 Full HDTV format and can display 16.7M colors (8-bit). The backlight unit is not built in.

1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Pixels [lines]	1920 × 641
Active Area [mm]	878.112(H) x289.4(V)
Pixel Pitch [mm]	0.15245 (H) x 0.4494 (V)
Pixel Arrangement	RGB Vertical Stripe
Weight [g]	TBD Typ. (g)
Overall dimensions [mm]	901.6(H)x313.3(V)x15.69(D) (Typ)
Display Mode	Transmissive Mode / Normallly Black
Contrast Ratio	Typ.5000:1 (Typical value measure by INX's Module)
Glass thickness (Array / CF) [mm]	0.5 / 0.5
Viewing Angle (CR>10) (VA model)	Typ. +89/-89(H), +89/-89(V) (CR≧10) (Typical value measured by INX's module)
Color Chromaticity	R = (0.6524,0.3265) G = (0.3266,0.6119) B = (0.1455,0.0555) W= (0.2837,0.2973) * Please refer to "color chromaticity" in 6.2
Cell Transparency [%]	6.0% Typ. Please refer to "Transmittance" in 6.2
Polarizer Surface Treatment	AG (Haze~1%) Hardness: 3H
Rotation Function	Unachievable
Display Orientation	Signal input with "INX"
RoHs Compliance	

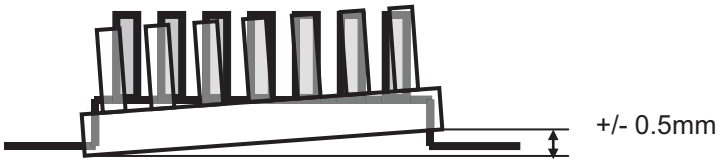


1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	TBD	TBD	TBD	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ± 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1), (3)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2), (3)

Note (1) Temperature and relative humidity range is shown in the figure below.

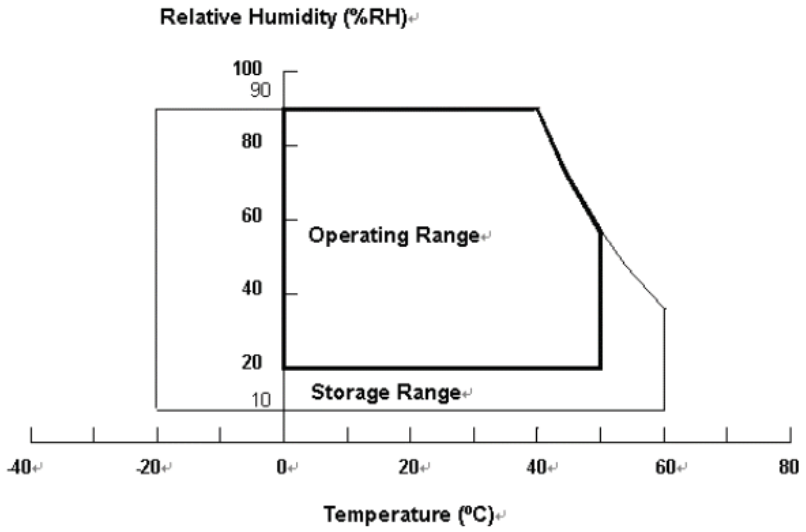
(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) The rating of environment is base on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.



2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

When storing open cell units, following procedures are necessary.

(1) Temperature : 5~40 ℃

(2) Humidity : 35~75%RH

(3) Period : 6 months

(4) Control of ventilation and temperature is necessary.

(5) Please make sure to protect the product from strong light exposure, water or moisture. Be careful for condensation.

(6) If products delivered or kept in conditions of the recommended temperature or humidity, we recommend you leave them at a circumstance which is shown as below.

Period	1 month	2 months	3 months	4 months	5 months	6 months
Baking condition	No baking		50℃, 10%, 24 hrs	50℃, 10%, 48 hrs		

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	
Component thermal	-	-	100	℃	(2)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) The surface temperature of Source Driver and component on PCB should be controlled under 100℃ operating over thermal spec can cause the damage or decrease of lifetime.

2.4 BACKLIGHT UNIT

Parameter			Symbol	Values			Unit	notes
				Min	Typ	Max		
LED Driver :								
Power Supply Input Voltage			VBL	21.6	24.0	24.5	Vdc	1
Power Supply Input Current			IBL	-	0.83	1.02	A	1
Power Supply Input Current (In-Rush)			In-rush	-	-	(TBD)	A	V_{BL} = 24.0V $ExtV_{BR-B}$ = 100% 3
Power Consumption			PBL	-	20	25	W	1
Input Voltage for Control System Signals	On/Off	On	V on	2.5	-	5.5	Vdc	
		Off	V off	-0.3	0.0	0.5	Vdc	
	Brightness Adjust		$ExtV_{BR-B}$	30	-	100	%	On Duty 5
				30	-	100	%	
	$ExtV_{BR-B}$ Frequency		f_{PWM}	500	-	1500	Hz	
	Pulse Duty Level (PWM)		High Level	2.5	-	5.5	Vdc	HIGH : on duty LOW : off duty
			Low Level	0.0	-	0.5	Vdc	
LED :								
Life Time				30,000	50,000		Hrs	2

notes :

1. Electrical characteristics are determined after the unit has been 'ON' and stable for approximately 60 minutes at 25±2°C. The specified current and power consumption are under the typical supply Input voltage 24Vand V_{BR} ($ExtV_{BR-B}$: 100%), it is total power consumption.
2. The life time (MTTF) is determined as the time which luminance of the LED is 50% compared to that of initial value at the typical LED current (ExtVBR-B :100%) on condition of continuous operating in LCM state at 25±2°C.
3. The duration of rush current is about 200ms. This duration is applied to LED on time.
4. Even though inrush current is over the specified value, there is no problem if I^2T spec of fuse is satisfied. $ExtV_{BR-B}$ signal have to input available duty range and sequence.
5. After Driver ON signal is applied, $ExtV_{BR-B}$ should be sustained from 30% to 100% more than 500ms. After that, $ExtV_{BR-B}$ 30% and 100% is possible

2.5 LIGHTBAR Connector Pin Assignment

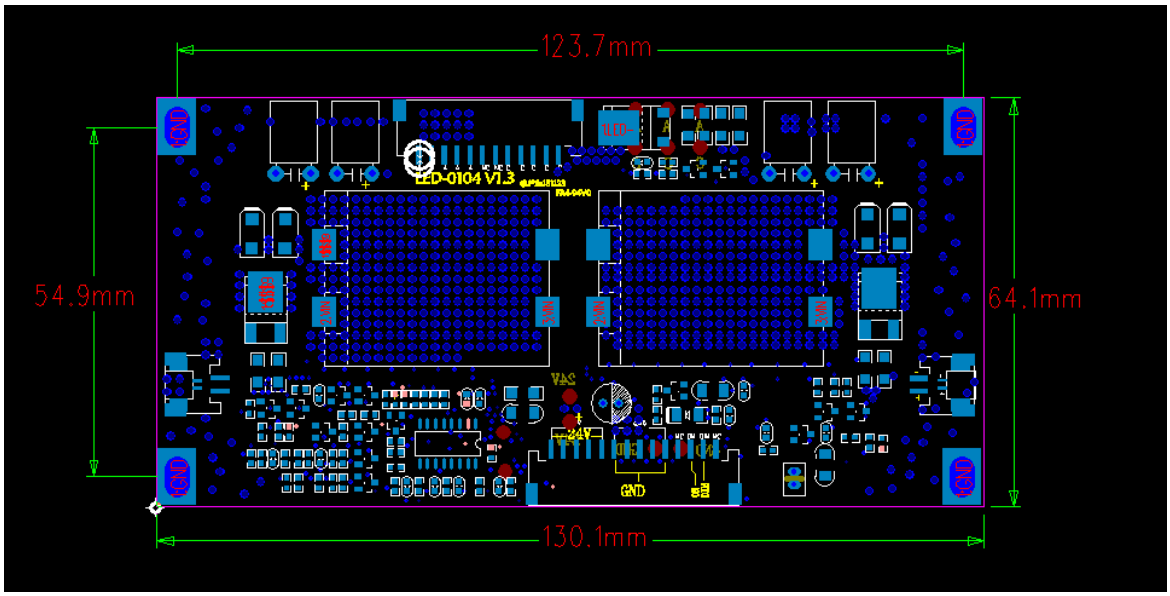


Table 4-2(CN2):Input terminal PH2.0-14(2.0mmX14)

PIN #	Symbol	Description
1	V_{DDB}	Operating Voltage Supply, +24V DC Regulated
2	V_{DDB}	Operating Voltage Supply, +24V DC Regulated
3	V_{DDB}	Operating Voltage Supply, +24V DC Regulated
4	V_{DDB}	Operating Voltage Supply, +24V DC Regulated
5	V_{DDB}	Operating Voltage Supply, +24V DC Regulated
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11		Not connect
12	VBLON	BL On-Off: High (2.5~5.5V) for BL , Low/Open (0~0.5V) for BL **off**
13	VDIM (note 1)	**Internal PWM Dimming** High (5.5V/100% Duty) for 100% Lum; <NC; when external PWM>
14		Not connect

Note (1) PWM dimming function is included internal PWM and external PWM. Internal PWM: input voltage 0 (GND) ~5.5V to pin 13th, and duty ratio of output voltage/current of inverter is from 30% to 100%. When use pin 13th to control backlight luminance, the pin 14th will be NC .

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD OPEN CELL

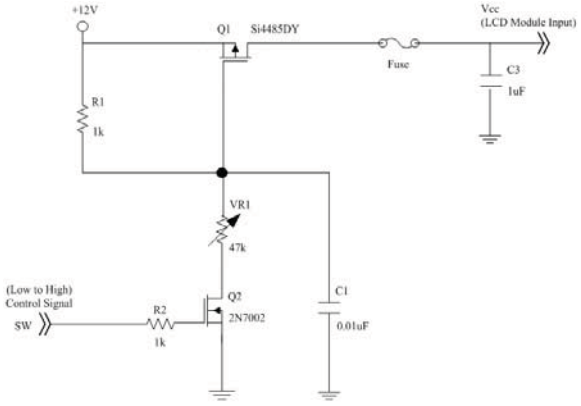
(Ta = 25 ± 2 °C)

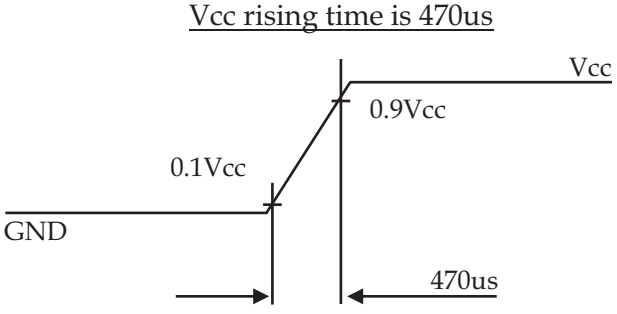
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	—	—	2.58	A	(2)
Power Consumption	White Pattern	P_T	—	4.71	5.18	W	(3)
	Black Pattern	P_T	—	4.25	4.48	W	
	Horizontal Stripe	P_T	—	5.94	6.53	W	
Power Supply Current	White Pattern	—	—	0.40	0.48	A	
	Black Pattern	—	—	0.36	0.44	A	
	Horizontal Stripe	—	—	0.52	0.61	A	
LVDS interface	Differential Input High Threshold Voltage	V_{TH}	—	—	+100	mV	(4)
	Differential Input Low Threshold Voltage	V_{TL}	-100	—	—	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$\|V_{ID}\|$	100	—	600	mV	
	Terminating Resistor	R_T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

The ripple voltage should be controlled under 10% of Vcc (Typ.).

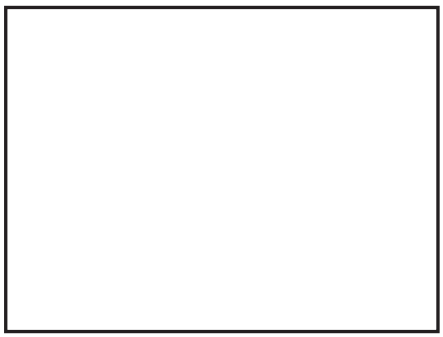
Note (2) Measurement condition :





Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 °C, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

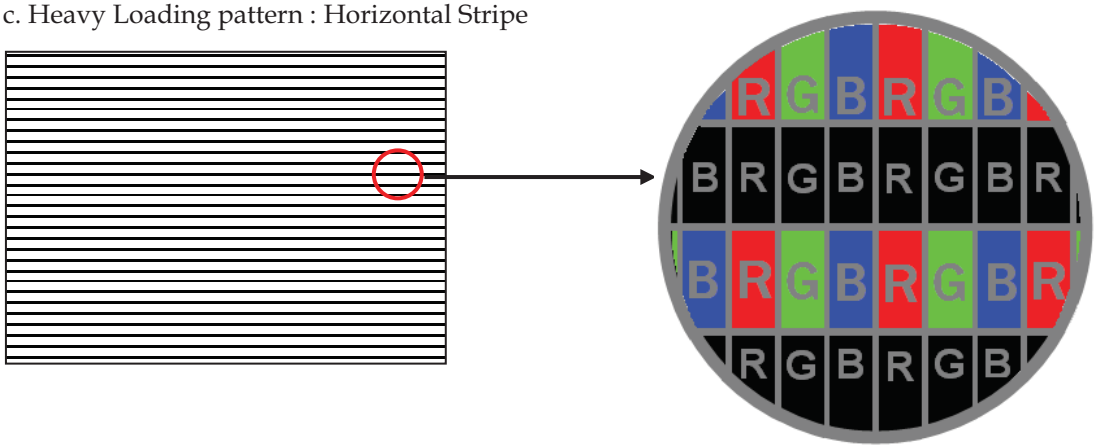


Active Area

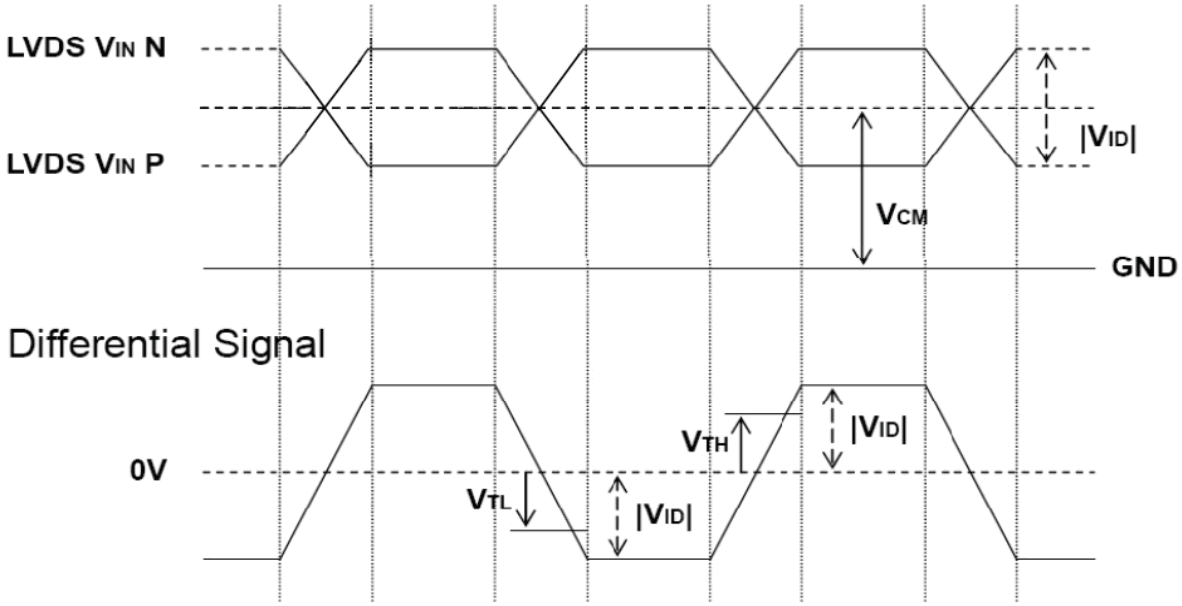
b. Black Pattern

Active Area

c. Heavy Loading pattern : Horizontal Stripe



Note (4) The LVDS input characteristics is shown as below. The position of measurement is TCON LVDS input pin. The differential voltage must be higher than VTH and lower than VTL to ensure that the receiver indicates a valid logic state at its output.



4. INPUT TERMINAL PIN ASSIGNMENT

4.1 TFT LCD OPEN CELL

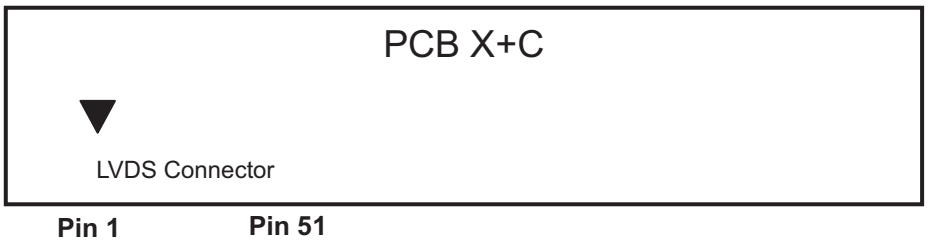
CNF1 Connector Pin Assignment: [187059-51221 (P-Two), WF23-402-5133(FCN)]

Matting connector : [FI-RE51HL(JAE)]

Pin	Name	Description	Note
1	NC	No connection	(2)
2	SCL	I2C clock (For Vcom tunning)	
3	SDA	I2C data (For Vcom tunning)	
4	NC	No connection	(2)
5	NC	No connection	
6	NC	No connection	
7	SELLVDS	LVDS data format Selection	(3)(4)
8	NC	No Connection	(2)
9	NC	No Connection	
10	NC	No connection	
11	GND	Ground	
12	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(5)
13	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
14	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
15	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
16	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
17	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	Odd pixel Negative LVDS differential clock input.	(5)
20	OCLK+	Odd pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(5)
23	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	(2)
25	N.C.	No Connection	
26	N.C.	No Connection	
27	N.C.	No Connection	
28	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(5)
29	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
30	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
31	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
32	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
33	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	Even pixel Negative LVDS differential clock input	(5)
36	ECLK+	Even pixel Positive LVDS differential clock input	
37	GND	Ground	
38	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(5)
39	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	(2)
41	N.C.	No Connection	
42	N.C.	No Connection	
43	N.C.	No Connection	
44	GND	Ground	
45	GND	Ground	

46	GND	Ground	
47	N.C.	No Connection	(2)
48	VCC	Power input (+12V)	
49	VCC	Power input (+12V)	
50	VCC	Power input (+12V)	
51	VCC	Power input (+12V)	

Note (1) LVDS connector pin orderdefined as below



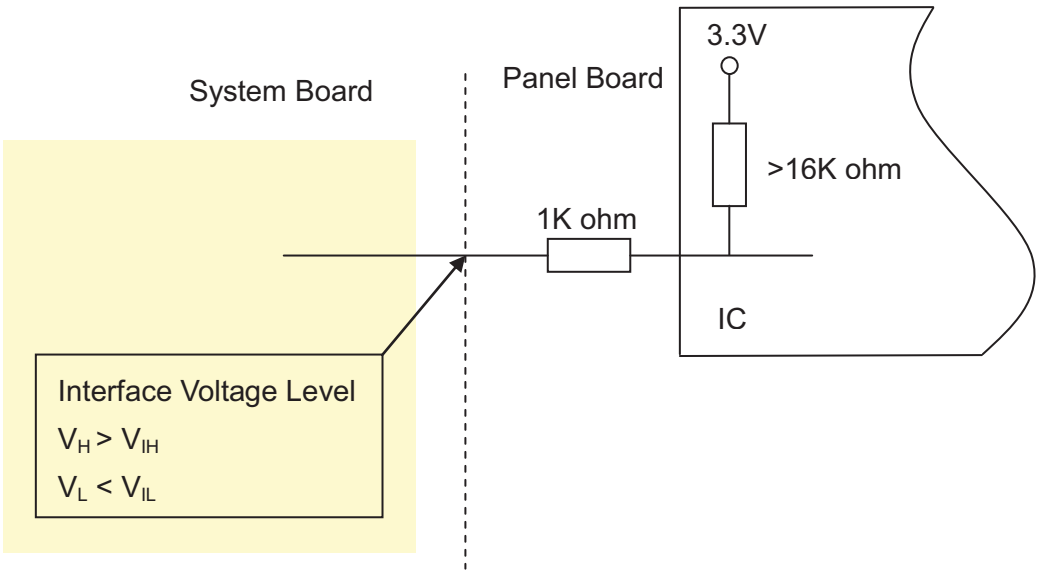
Note (2) Reserved for internal use. Please leave it open.

Note (3) Connect to Open or +3.3V: VESA Format, connect to GND: JEIDA Format.

SELLVDS	Mode
H(default)	VESA
L	JEIDA

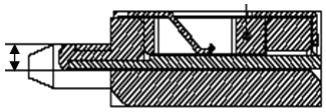
L : Connect to GND, H: Connect to +3.3V

Note (4) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including Panel board loading as below.

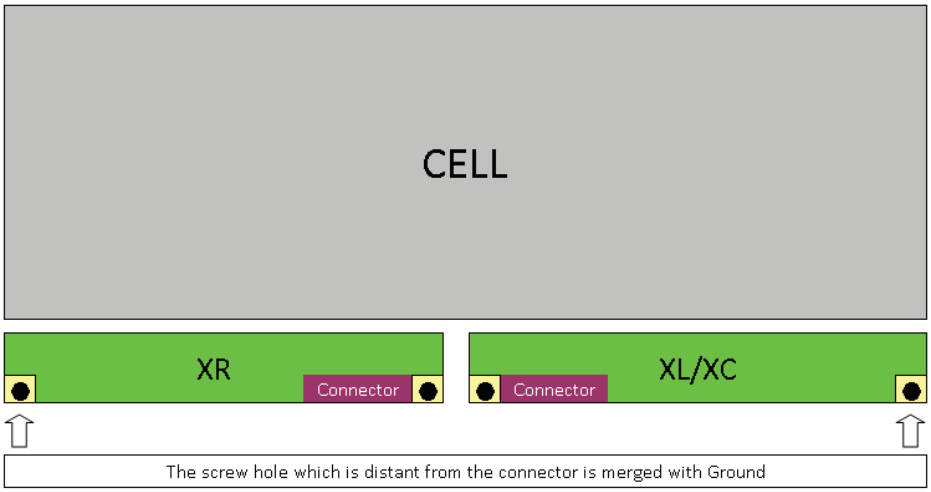


Note (5) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

Note (6) LVDS connector mating dimension range request is 0.93mm~1.0mm as below.



Note (7) The screw hole which is distant from the connector is merged with Ground.

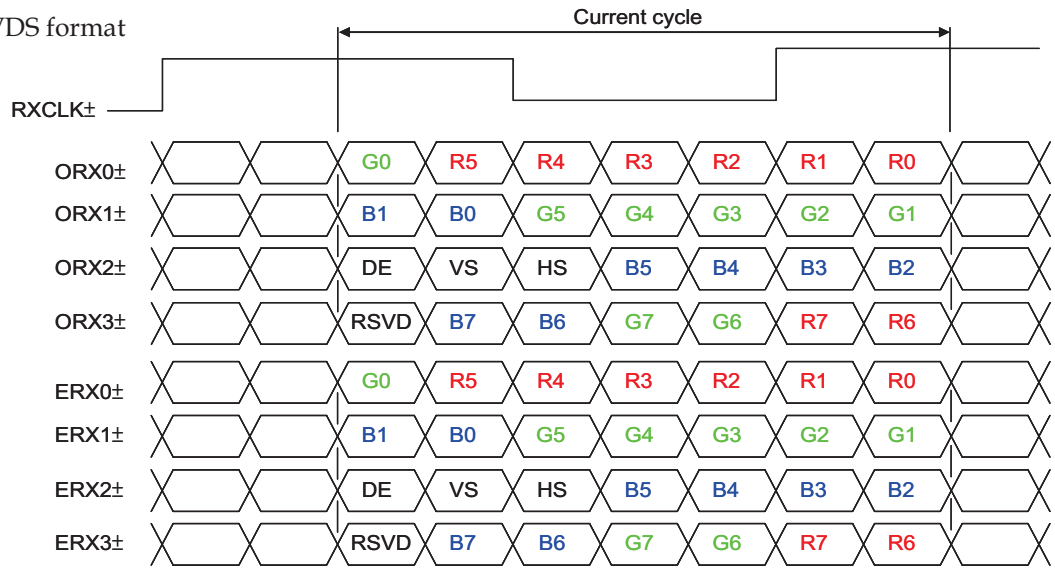


4.2 LVDS INTERFACE

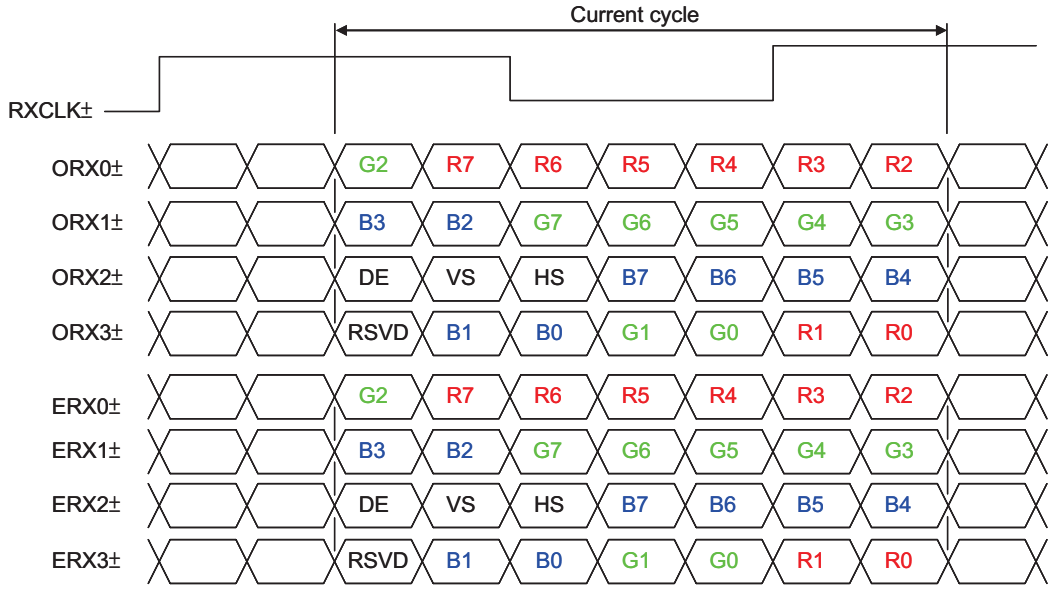
JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open

VESA LVDS format



JEDIA LVDS format



R0~R7	Pixel R Data (7; MSB, 0; LSB)	DE	Data enable signal
G0~G7	Pixel G Data (7; MSB, 0; LSB)	DCLK	Data clock signal
B0~B7	Pixel B Data (7; MSB, 0; LSB)		

Note (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

4.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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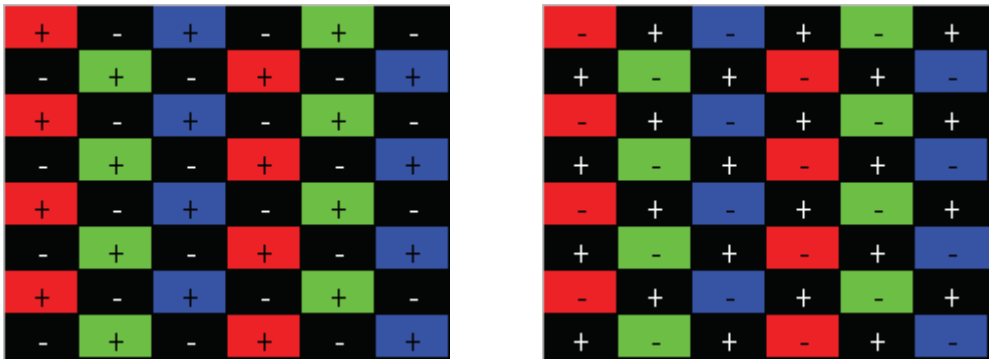
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

4.4 FLICKER (Vcom) ADJUSTMENT

(1) Adjustment Pattern :

The adjustment pattern is shown as below. If customer needs below pattern, please directly contact with account FAE.



(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. INX provide Auto Vcom tools to adjust Digital V-com.The detail connection and setting instruction, please directly contact with Account FAE or refer INX Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.

a. USB Sensor Board.

b. Programmable software

5. INTERFACE TIMING

5.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

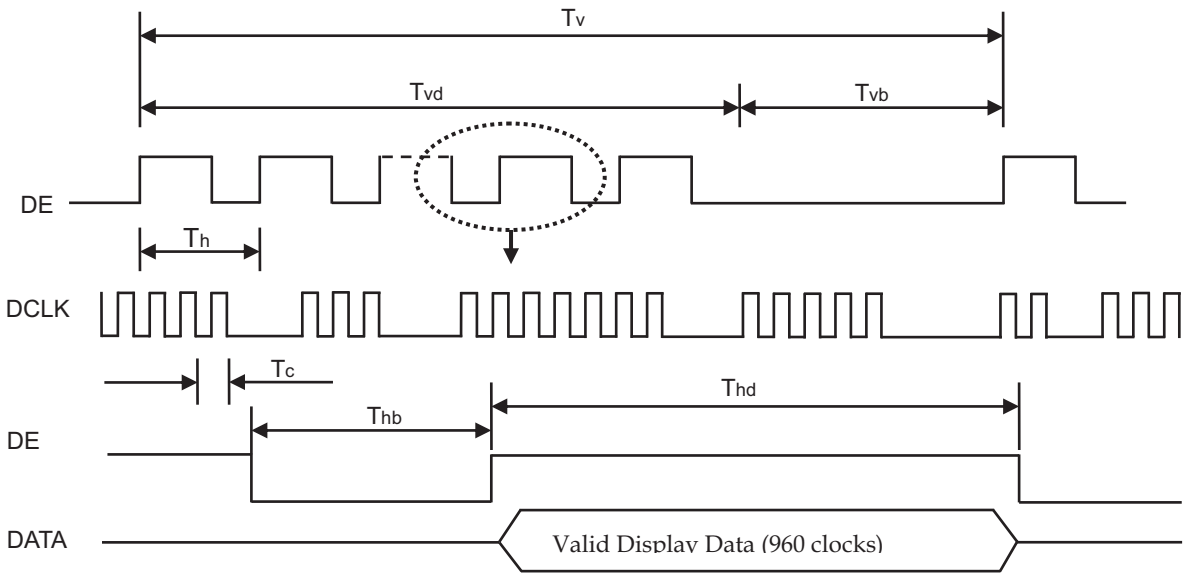
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	—	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	—	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	—	—	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSKM}	-400	—	400	ps	(5)
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	(6)
		F_{r6}	57	60	63	Hz	
	Total	Tv	1110	1125	1480	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	—
	Blank	Tvb	20	45	400	Th	—
Horizontal Active Display Term	Total	Th	1030	1100	1325	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	—
	Blank	Thb	70	140	365	Tc	—

Note (1) Please make sure the range of pixel clock has follow the below equation :

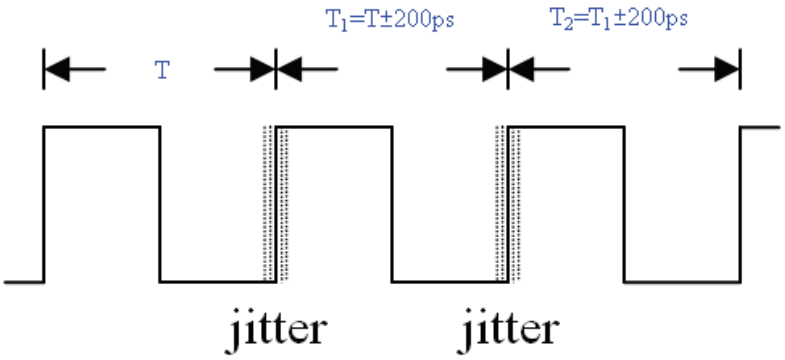
Fclkin(max) ≧ Fr6 × Tv × Th

Fr5 × Tv × Th ≧ Fclkin (min)

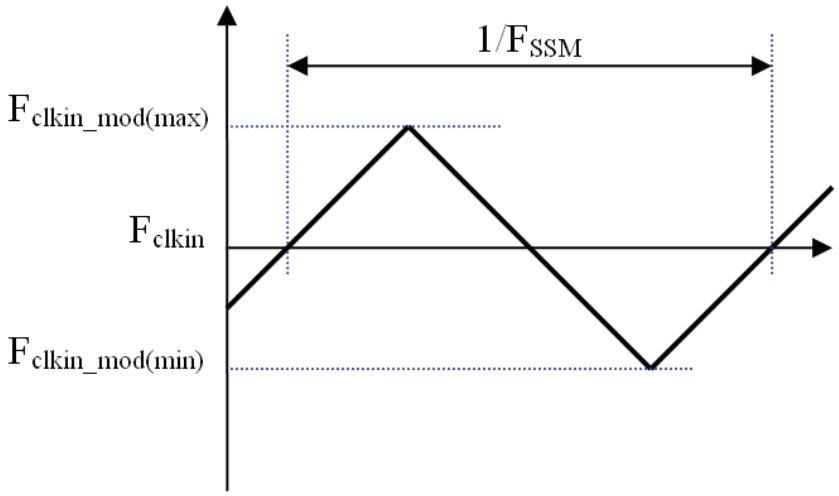
Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below :



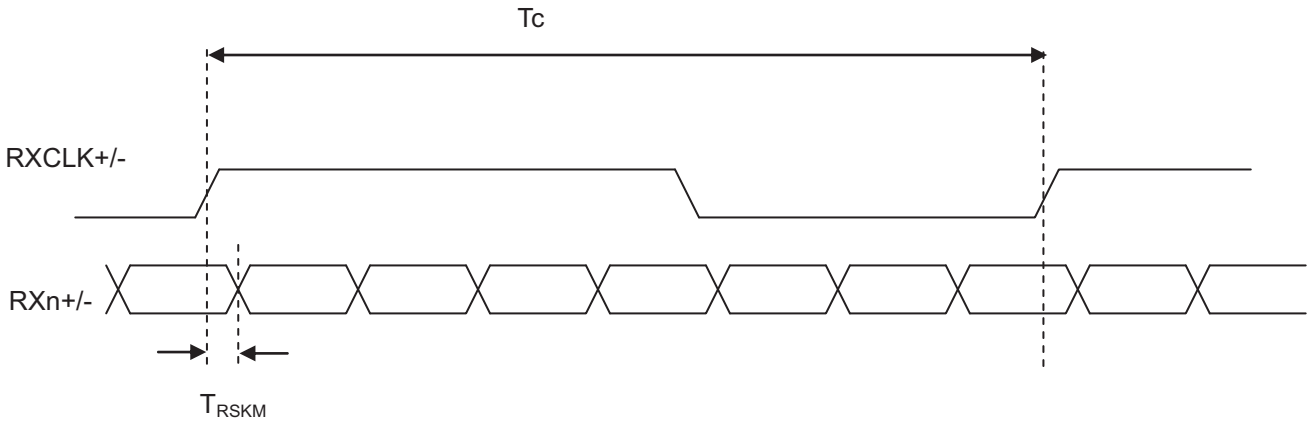
Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = | T_1 – T |



Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



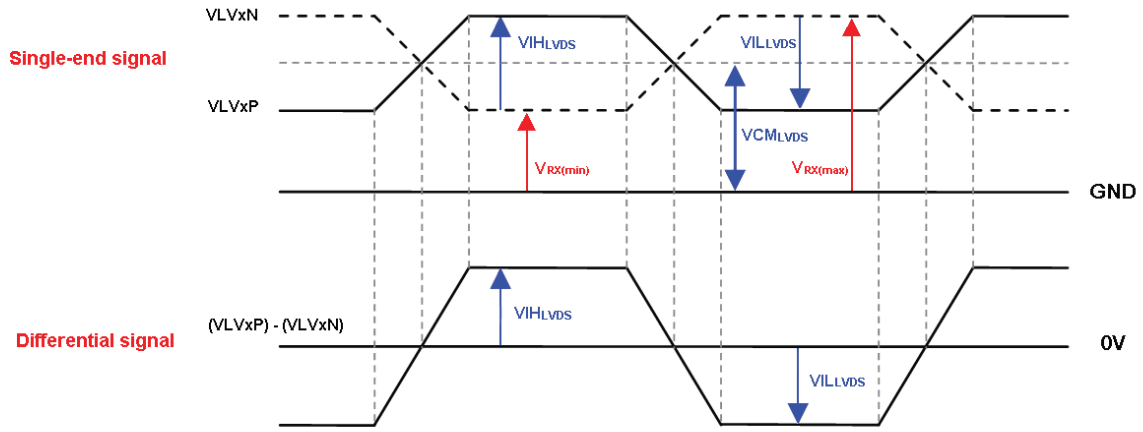
Note (5) The LVDS timing diagram and the receiver skew margin is defined and shown in following figure.

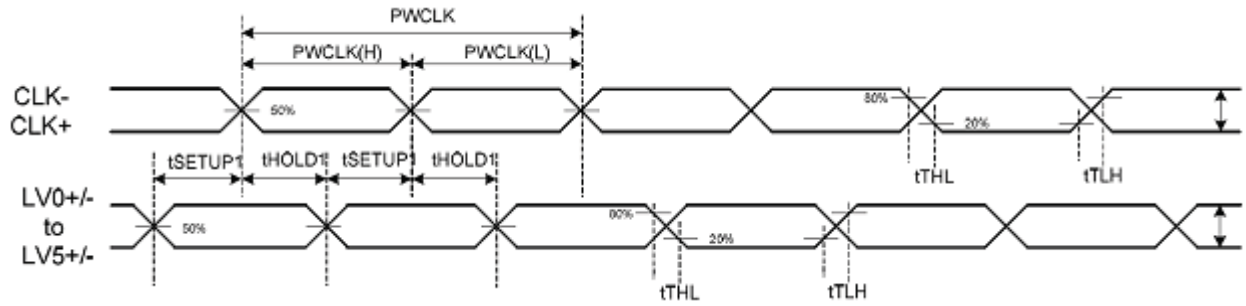


5.2 INTRA INTERFACE SIGNAL TIMING SPECIFICATIONS

5.2.1 Mini-LVDS Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
mini-LVDS power Voltage	VDD	2.3	3.3	3.6	V	
mini-LVDS high input voltage	|VIHLVDS|	175	-	-	mV	Fmax ≦ 340MHz
mini-LVDS low input voltage	|VILLVDS|	175	-	-	mV	Fmax ≦ 340MHz
mini-LVDS input voltage range	VRX	0	-	VDD	V	
mini-LVDS common mode input voltage range	VCMLVDS	0.5	1.2	VDD-1.2	V	VCMLVDS = (VCLKP + VCLKN) / 2 or VCMLVDS = (VLVxP + VLVxN) / 2
Data setup time	tSETUP1	0.45	-	-	ns	
Data hold time	tHOLD1	0.45	-	-	ns	
CLK Rising Time	tTLH	-	-	0.7	Ns	From VILLVDS to VIHLVDS
CLK Falling Time	tTHL	-	-	0.7	ns	From VIHLVDS to VILLVDS





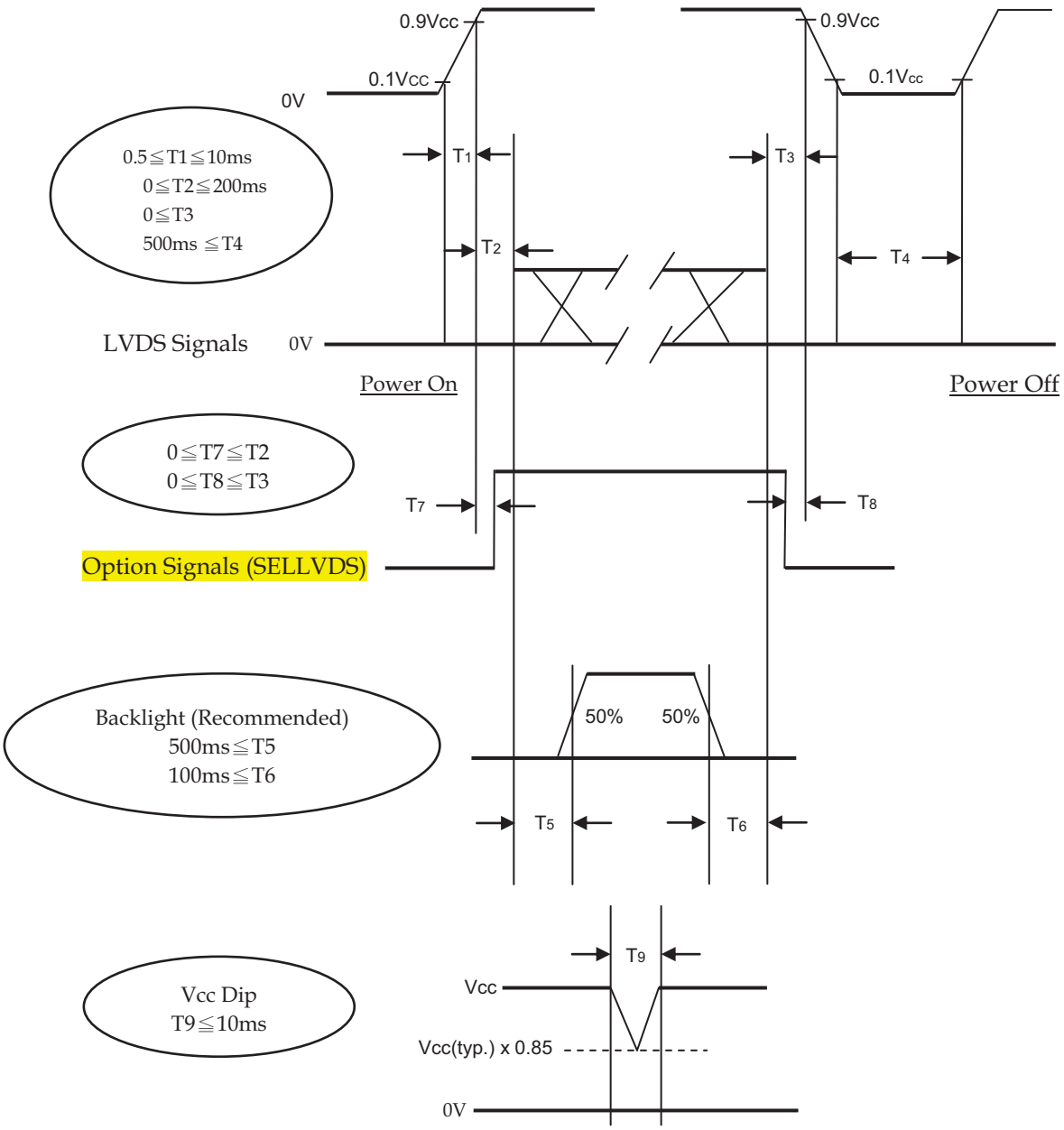
Notes:

(1) EYE diagram must meet above spec. Data receiver is not gauranteed If EYE diagram is smaller than spec.

(2) Measure point : Pads of XR-board terminal resistances RX3, RX4, RX5, RX6, and Pads of XC-board terminal resistances RX15, RX16, RX17, RX18

5.3 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.
If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

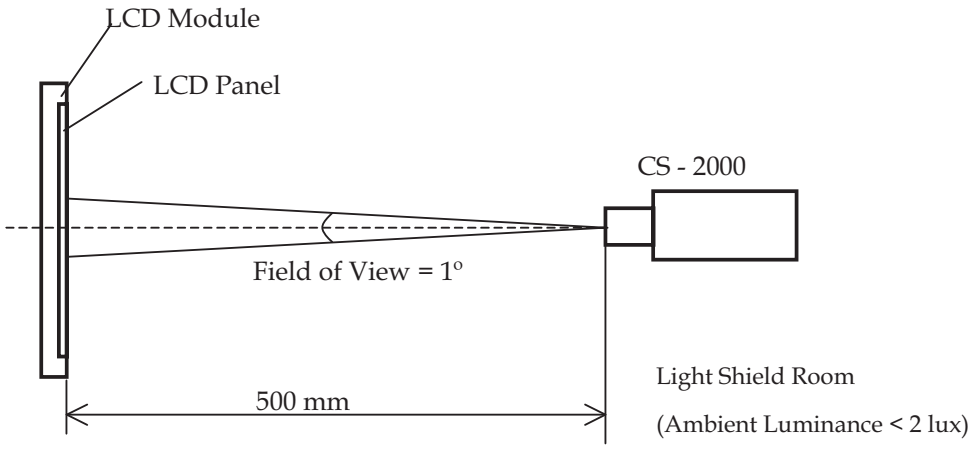
Note (6) Vcc must decay smoothly when power-off.

6. OPTICAL CHARACTERISTICS

6.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25 ±2	°C
Ambient Humidity	Ha	50 ±10	%RH
Vertical Frame Rate	Fr	60	Hz
Supply Voltage	V_{CC}	12.0 ±1.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



6.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 6.1 and stable environment shown in 6.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	θ_x=0°, θ_Y =0° Viewing Angle at Normal Direction Standard light source "C"	-0.03	0.6524	+0.03	-	(0)
		Rcy			0.3265		-	
	Green	Gcx			0.3266		-	
		Gcy			0.6119		-	
	Blue	Bcx			0.1455		-	
		Bcy			0.0555		-	
	White	Wcx			0.2837		-	
		Wcy			0.2973		-	
Transmittance		T%	θ_x=0°, θ_Y =0° With INX Module@60Hz	5.4	6.0	-	%	(5)
Transmittance Variation		δT		-	-	1.3		(6)
Contrast Ratio		CR		3500	5000	-	-	(1), (3)
Response Time		Gray to gray	θ_x=0°, θ_Y =0° With INX Module@60Hz	-	9.5	18	ms	(1), (4)
Viewing Angle	Horizontal	θ_x+	CR≥10 With INX Module	80	89	-	Deg.	(1), (2)
		θ_x-		80	89	-		
	Vertical	θ_Y+		80	89	-		
		θ_Y-		80	89	-		
brightness				450	500	-	cd/m^2	

Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following :

1.Measure Module's and BLU's spectrum at center point. W, R,G, B are with signal input. BLU (V400DJ1-KS5) is supplied by INX.

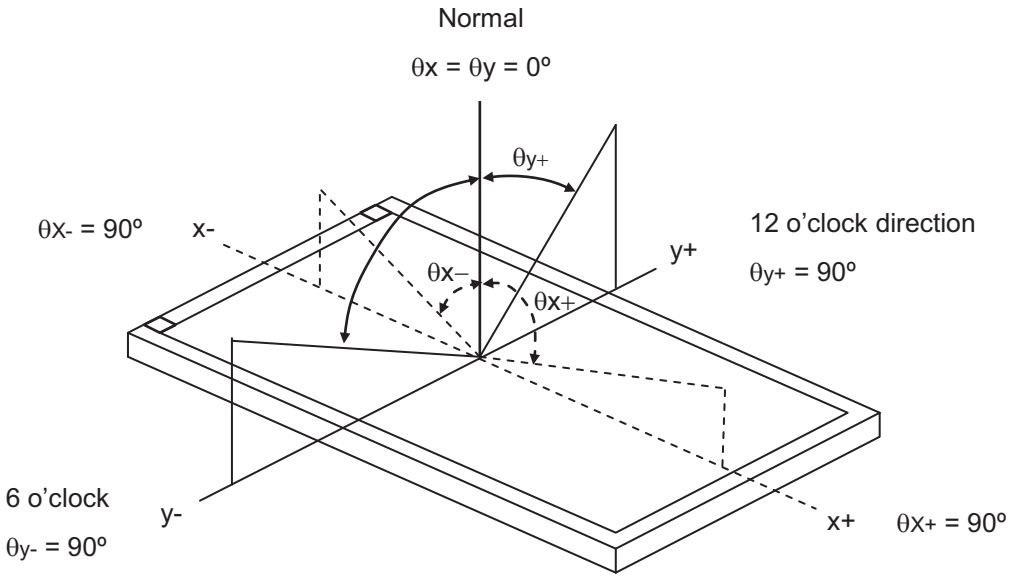
2.Calculate cell's spectrum.

3.Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which supplied by INX ((V400DJ1-KS5) and the cell driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R)



Note (3) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

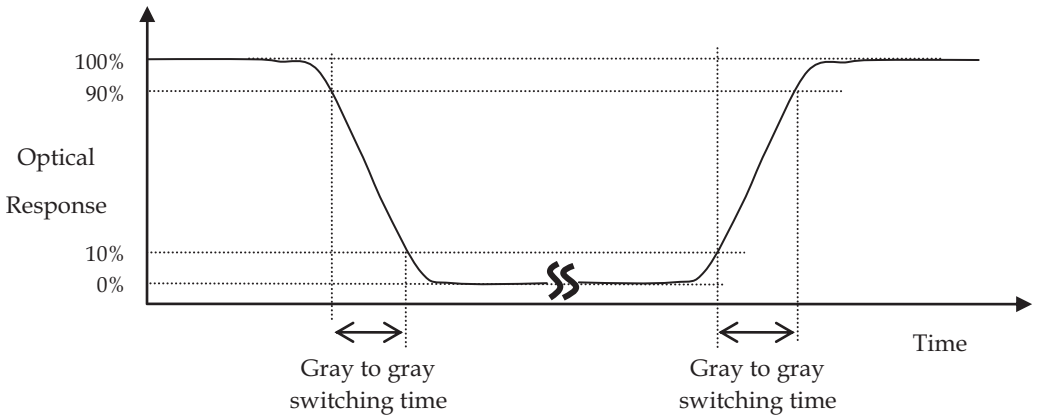
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (4) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255.

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255 to each other.

Note (5) Definition of Transmittance (T%) :

Measure the transmittance at 5 points.

Light source is the BLU which contains three diffuser sheets and the cell driving voltage are based on suitable gamma voltages.

Transmittance (T%) = $\text{Average}\left[T(1), T(2), T(3), T(4), T(5)\right]$

The transmittance of each point can be calculated by the following expression.

$$T(X) = \frac{L255\,(X) \text{ of LCD module}}{\text{Luminance (X) of BLU}} \times 100\%$$

L255: Luminance of gray level 255

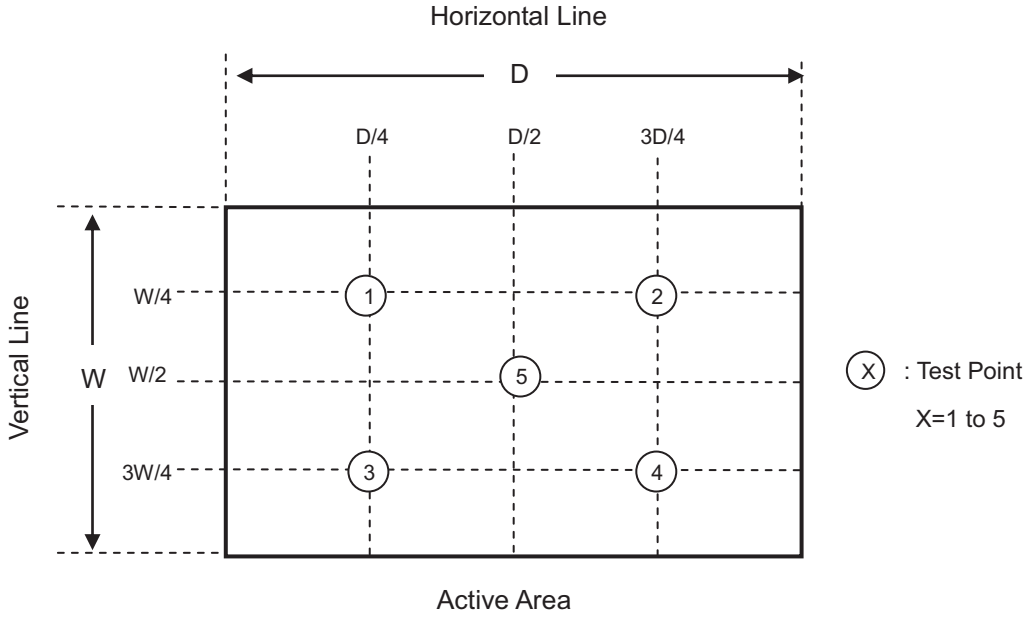
T(X) is corresponding to the point X1~X5 at the figure in Note (6).

Note (6) Definition of Transmittance Variation (δT) :

Measure the transmittance at 5 points.

$$\text{Transmittance Variation } (\delta T) = \frac{\text{Maximum}[\,T(1), T(2), T(3), T(4), T(5)\,]}{\text{Minimum}[\,T(1), T(2), T(3), T(4), T(5)\,]}$$

T(X) is calculated as Note(5).



7. PRECAUTIONS

7.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply improper or unbalanced force such as bending or twisting to open cells during assembly.

[2] It is recommended to assemble or to install an open cell into a customer's product in clean working areas. The dust and oil may cause electrical short to an open cell or worsen polarizers on an open cell.

[3] Do not apply pressure or impulse to an open cell to prevent the damage.

[4] Always follow the correct power-on sequence when an open cell is assembled and turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] Do not design sharp-pointed structure / parting line / tooling gate on the plastic part of a COF (Chip on film), because the burr will scrape the COF.

[6] If COF would be bended in assemble process, do not place IC on the bending corner.

[7] The gap between COF IC and any structure of BLU must be bigger than 2 mm. This can prevent the damage of COF IC.

[8] The bezel opening must have no burr and be smooth to prevent the surface of an open cell scraped.

[9] The bezel of a module or a TV set can not contact with force on the surface of an open cell. It might cause light leakage or scrape.

[10] In the case of no FFC or FPC attached with open cells, customers can refer the FFC / FPC drawing and buy them by self.

[11] It is important to keep enough clearance between customers' front bezel/backlight and an open cell. Without enough clearance, the unexpected force during module assembly procedure may damage an open cell.

[12] Do not plug in or unplug an I/F (interface) connector while an assembled open cell is in operation.

[13] Use a soft dry cloth without chemicals for cleaning, because the surface of the polarizer is very soft and easily scratched.

[14] Moisture can easily penetrate into an open cell and may cause the damage during operation.

[15] When storing open cells as spares for a long time, the following precaution is necessary.

[15.1] Do not leave open cells in high temperature and high humidity for a long time. It is highly recommended to store open cells in the temperature range from 0 to 35℃ at normal humidity without condensation.

[15.2] Open cells shall be stored in dark place. Do not store open cells in direct sunlight or fluorescent light environment.

[16] When ambient temperature is lower than 10ºC, the display quality might be reduced.

[17] Unpacking (Cartons/Tray plates) in order to prevent open cells broken:

[17.1] Moving tray plates by one operator may cause tray plates bent which may induce open cells broken. Two operators carry one carton with their two hands. Do not throw cartons/tray plates, avoid any impact on cartons/tray plates, and put down & pile cartons/tray plates gently.

[17.2] A tray plate handled with unbalanced force may cause an open cell damaged. Trays should be completely put on a flat platform.

[17.3] To prevent open cells broken, tray plates should be moved one by one from a plastic bag.

[17.4] Please follow the packing design instruction, such as the maximum number of tray stacking to prevent the deformation of tray plates which may cause open cells broken.

[17.5] To prevent an open cell broken or a COF damaged on a tray, please follow the instructions below:

[17.5.1] Do not peel a polarizer protection film of an open cell off on a tray

[17.5.2] Do not install FFC or LVDS cables of an open cell on a tray

[17.5.3] Do not press the surface of an open cell on a tray.

[17.5.4] Do not pull X-board when an open cell placed on a tray.

[18] Unpacking (Hard Box) in order to prevent open cells broken:

[18.1] Moving hard boxes by one operator may cause hard boxes fell down and open cells broken by abnormal methods. Two operators carry one hard box with their two hands. Do handle hard boxes carefully, such as avoiding impact, putting down, and piling up gently.

[18.2] To prevent hard boxes sliding from carts and falling down, hard boxes should be placed on a surface with resistance.

[18.3] To prevent an open cell broken or a COF damaged in a hard box, please follow the instructions below:

[18.3.1] Do not peel a polarizer protection film of an open cell off in a hard box.

[18.3.2] Do not install FFC or LVDS cables of an open cell in a hard box.

[18.3.3] Do not press the surface of an open cell in a hard box.

[18.3.4] Do not pull X-board when an open cell placed in a hard box.

[19] Handling – In order to prevent open cells, COFs , and components damaged:

[19.1] The forced displacement between open cells and X-board may cause a COF damaged. Use a fixture tool for handling an open cell to avoid X-board vibrating and interfering with other components on a PCBA & a COF.

[19.2] To prevent open cells and COFs damaged by taking out from hard boxes, using vacuum jigs to take out open cells horizontally is recommended.

[19.3] Improper installation procedure may cause COFs of an open cell over bent which causes damages. As installing an open cell on a backlight or a test jig, place the bottom side of the open cell first on the backlight or the test jig and make sure no interference before fitting the open cell into the backlight/the test jig.

[19.4] Handle open cells one by one.

[20] Avoid any metal or conductive material to contact PCB components, because it could cause electrical damage or defect.

[21] The suggestion of removing polarizer-protection film is illustrated as following

[21.1] Scan COF on the left side (Figure 1)

Remove slowly and follow the direction : from left-up to right-down

[21.2] Scan COF on the right side (Figure 2)

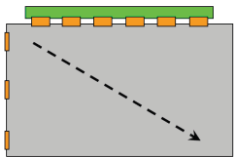
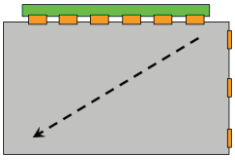
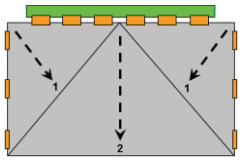
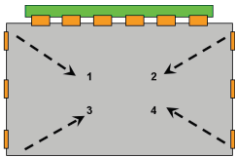
Remove slowly and follow the direction : from right-up to left-down

[21.3] Scan COF on the left and right side (Figure 3)

Remove slowly and follow the direction as marked by 1 and 2.

[21.4] Scan COF on the left and right side (Figure 4)

Remove slowly and follow the direction as marked by 1, 2, 3 and 4.

Figure 1	Figure 2	Figure 3	Figure 4
			

7.2 SAFETY PRECAUTIONS

[1] If the liquid crystal material leaks from the open cell, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[2] After the end of life, open cells are not harmful in case of normal operation and storage.

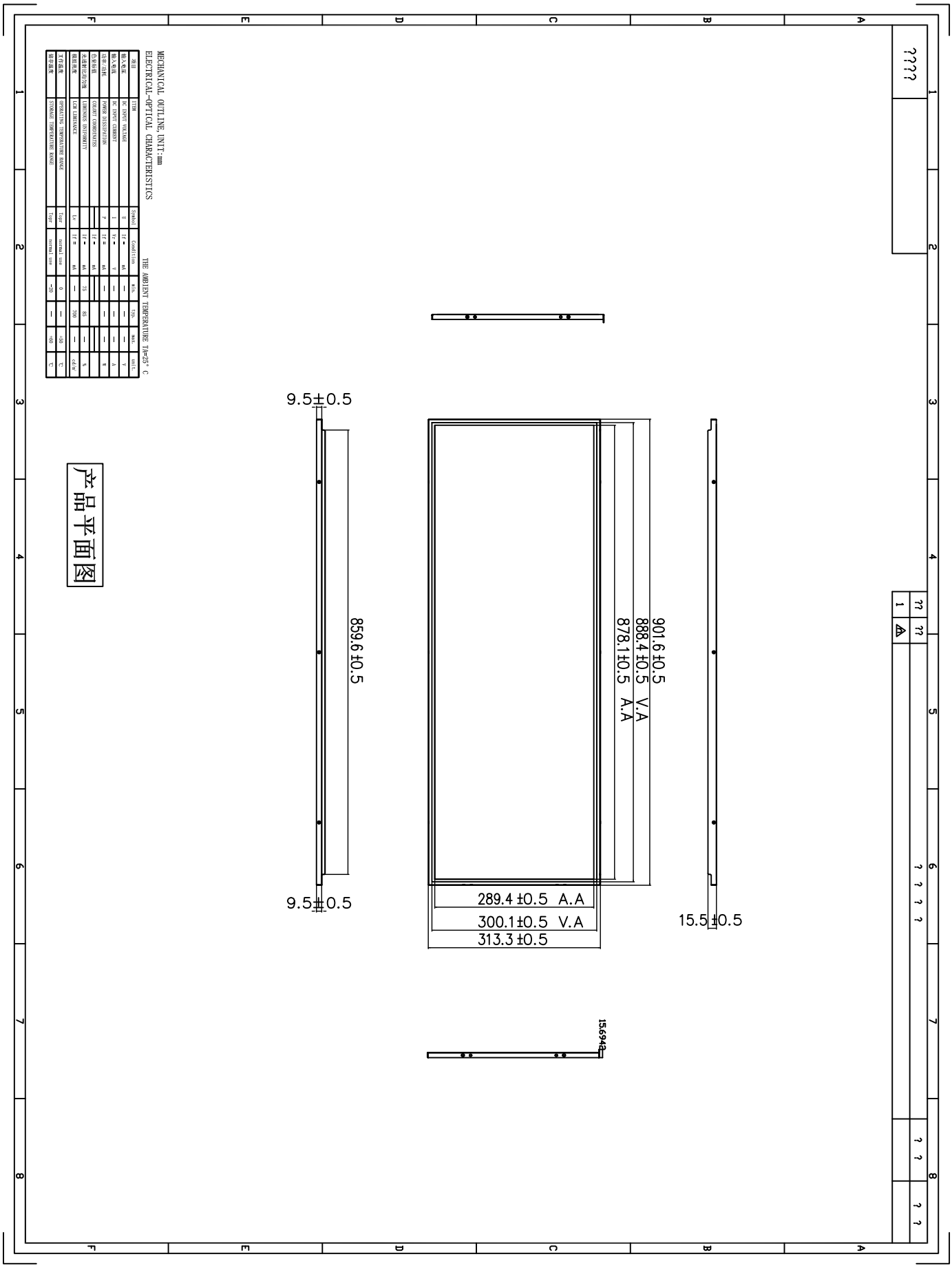
8. DEFINITION OF LABELS

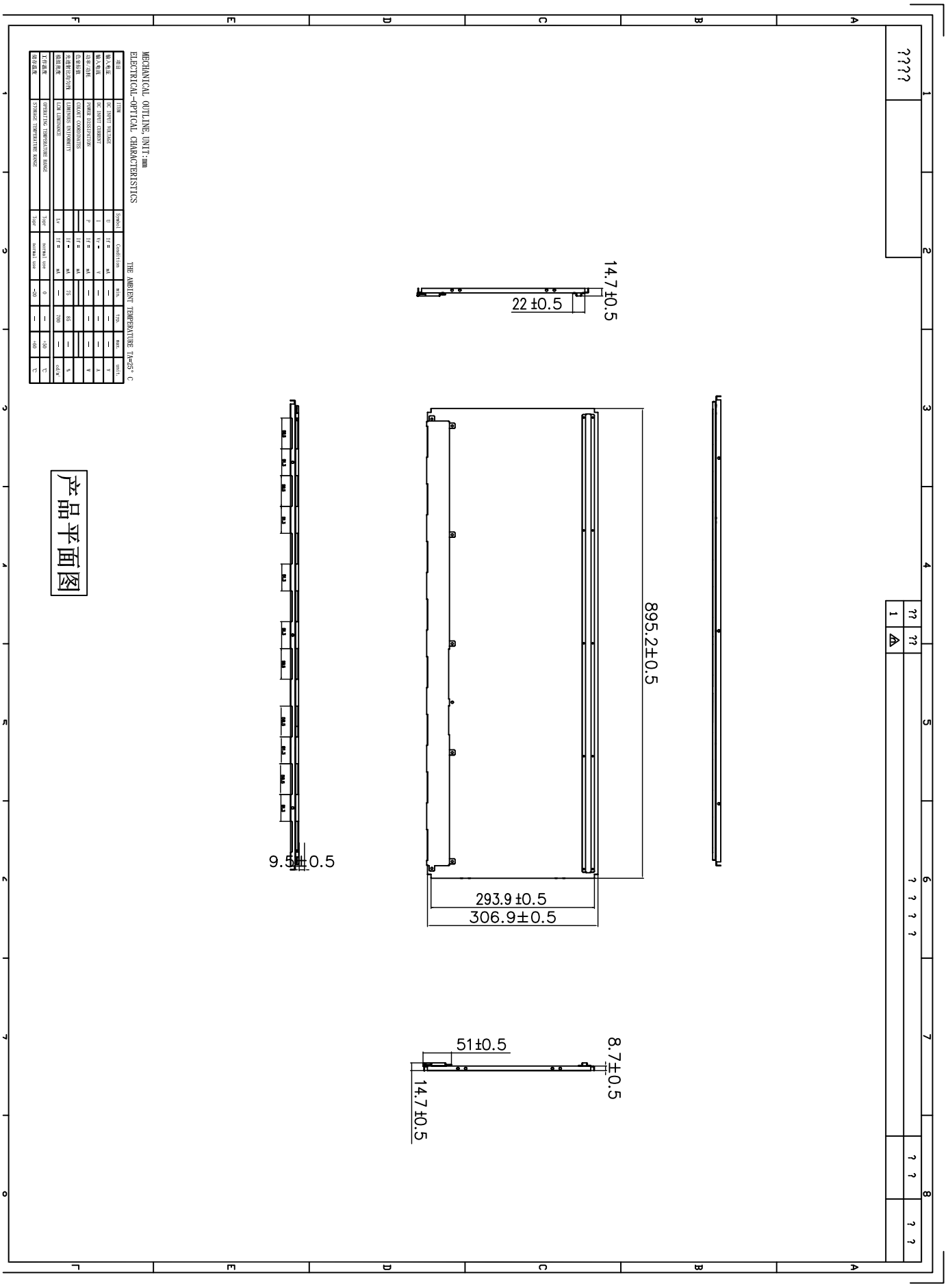
TBD

9. PACKAGING

TBD

10. MECHANICAL CHARACTERISTIC





MECHANICAL OUTLINE, UNIT: mm

ELECTRICAL-OPTICAL CHARACTERISTICS

THE AMBIENT TEMPERATURE TA=25° C

项目	ITEM		Symbol	Condition	MIN.	TYP.	MAX.	UNIT
输入电压	DC INPUT VOLTAGE		U	If =	4.5	—	—	V
输入电流	DC INPUT CURRENT		I	Vf =	—	—	A	
功率/功耗	POWER DISSIPATION		P	If =	mA	—	—	W
色坐标/色域	COLOUR COORDINATES			If =	mA			
色温解析度/均匀性	LUMINOUS UNIFORMITY			If =	mA			
亮度/发光	LCM LUMINANCE		Lv	If =	mA	75	85	—
工作温度	OPERATING TEMPERATURE RANGE		Topr	normal state	0	—	700	cd/㎡
储存温度	STORAGE TEMPERATURE RANGE		Tstr	normal state	-20	—	—	—
					—	—	—	+50
					—	—	—	+60
					—	—	—	°C

产品平面图