产 品 规 格 书

Product Specification

Model Name (产品名称)	TFT-LCD Module
Part Number (产品型号)	JT275FHI51R7L01

Item (项目)	Prepared (拟制)	Checked (审核)	Approved (批准)
Signature (签名)	HJL	ZQY	
Date (日期)	2025-12-22	2025-12-22	
Note (备注)			

Customer: (客户)

Signature (签名)	
Date (日期)	

Revision Record

Version	Issued Date	Page	Old Description	New Description
01	2025-12-22	\	Initial release	\

CONTENTS

1. General Description

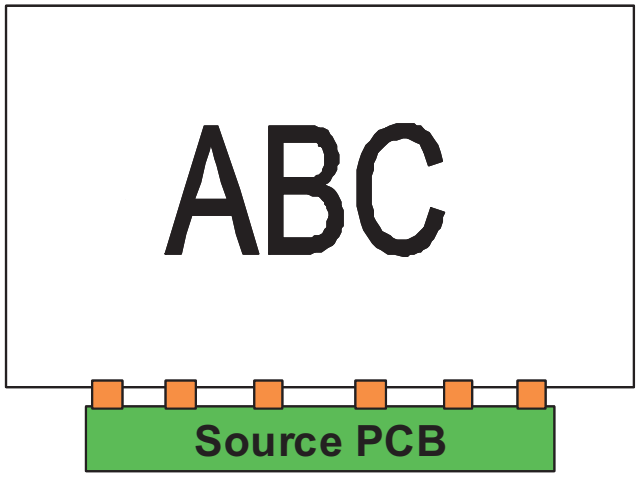
This specification applies to the 27.5 inch Color TFT-LCD SKD model. This Open Cell Unit has aTFT active matrix type liquid crystal panel with 1920 x 136 pixels and 8-bit 2 channel LVDS interface; which can display up to 16.7 million colors.

*** General Information**

Items	Specification	Unit	Note
Active Screen Size	27.5	inch	
Display Area	698.4(H) x 50(V)	mm	
Viewing area	702.4(H)X53(V)	mm	
Overall dimensions	714.4(H) x75(V)x19.2(D)	mm	
Driver Element	a-Si TFT active matrix		
brightness	700	cd/m^2	
Display Colors	8 bit (16.7 million)	Colors	
Number of Pixels	1,920 x 136	Pixel	
Pixel Pitch	0.36375 (H) x 0.36375(W)	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Surface Treatment	Anti-Glare, 3H		Haze=2%
Weight	TBD	kg	Typicalvalue
Display Orientation	Signal input with “ABC”		Note 1

Note 1: LCD display as below illustrated when signal input with “ABC”.

Front side



2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit or the unrecoverable damage on the device.

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V_{DD}	-0.3	14	[Volt] $_{DC}$	Note 1
Input Voltage of Signal	Vin	-0.3	4	[Volt]$_{DC}$	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	Note 3

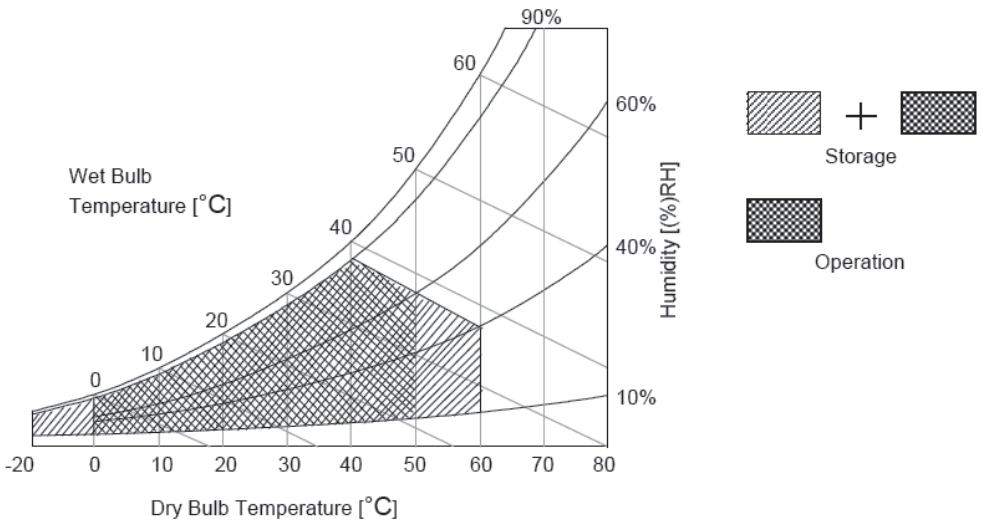
Note 1: Duration:50 msec.

Note 2 : Maximum Wet-Bulb should be 39℃ and No condensation.

The relative humi dity must not exceed 90 % non-condensing at temperatures of 40℃ or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃.

Note 3: Surface temperature is measured at 50℃ Dry condition

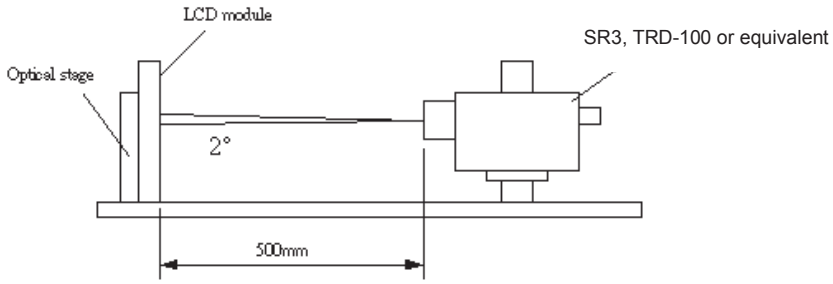
Note 4: These range above is maximumvalue not the actual operating temperature.Actual Operating temperature is no more than 50°C and temperature refers to the LCM surface temperature;Length of operation: No more than 8 hours per day, and no more than 4 hours of continuous use one time. It is recommended that the operating temperature be 0℃ to 50°C.



3. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25°C. The values specified are measured on the center of active area and at an approximate distance 500 mm from the LCD surface at a viewing angle of φ and θ equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



Parameter	Symbol	Condition	Values			Unit	Notes
			Min.	Typ.	Max		
Contrast Ratio	CR	SR3, TRD-100	3000	4000	--		1, 2
Response Time (G to G)	T_γ		--	8	16	ms	3
Color Chromaticity		With SR3 Standard light source "C"					4
Red	R_X		Typ.-0.03	0.6711	Typ.+0.03		
	R_Y			0.3193			
Green	G_X			0.3238			
	G_Y			0.6185			
Blue	B_X			0.1445			
	B_Y			0.0547			
White	W_X			0.2753			
	W_Y			0.2865			
Viewing Angle		SR3					1, 5
x axis, right(φ=0°)	θ_r		85	89	--	degree	
x axis, left(φ=180°)	θ_l		85	89	--	degree	
y axis, up(φ=90°)	θ_u		85	89	--	degree	
y axis, down (φ=270°)	θ_d		85	89	--	degree	
brightness			630	700	--	cd/m^2	

1. Light source here is the BLU of RX0275TA02 module (film structure: two diffuser sheets).
2. Contrast Ratio (CR) is defined mathematically as:

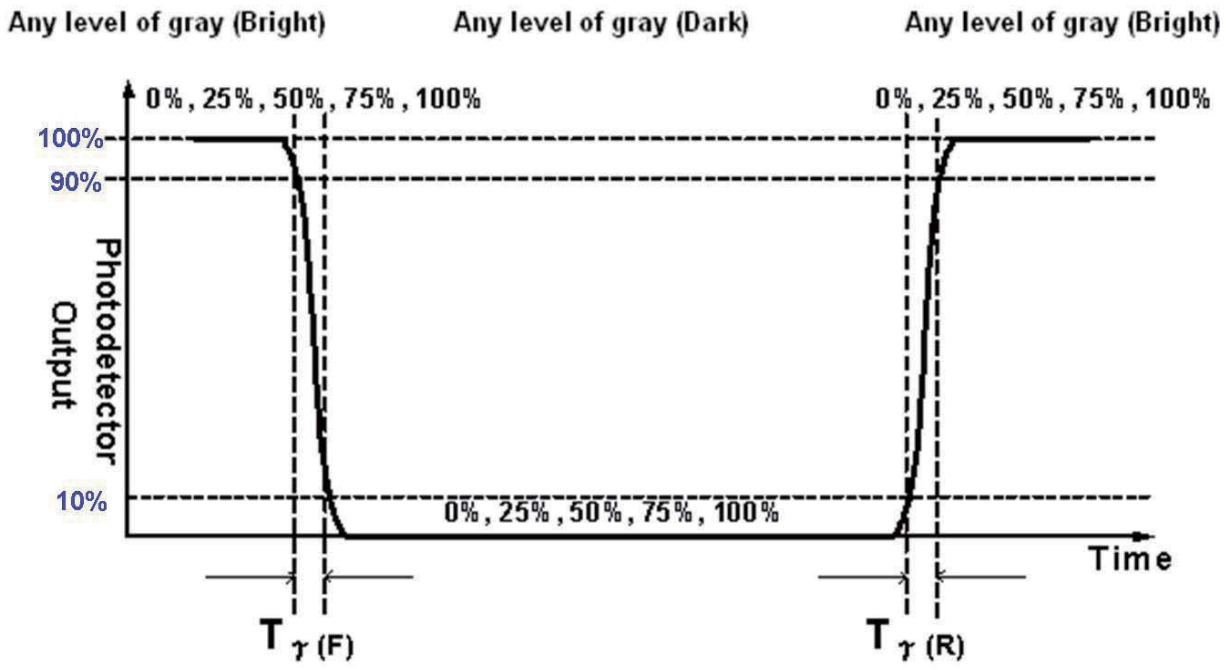
$$\text{Contrast Ratio} = \frac{\text{Surface Luminance at center location of all white pixels}}{\text{Surface Luminance at center location of all black pixels}}$$

3. Response time T_γ is the average time required for display transition by switc hing the input signal for five luminance ratio (0%,25%,50%,75%,100% brightness matrix) and is based on Frame rate = 60Hz to optimize.

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

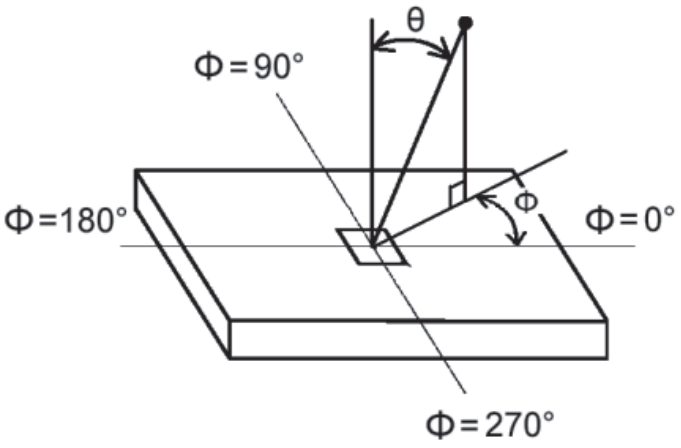
T_γ is determined by 10% to 90% brightness difference of rising or falling period. (As illustrated)
The response time is defined as the following figure and shall be measured by switching the input signal for "any level of gray(bright) " and "any level of gray(dark)".

FIG.3 Response Time



4. Light source here is the standard light source "C" which is defined by CIE and driving voltages are based on suitable gamma voltages. The calculating method is as following :
   A. Measure the "Module" and "BLU" optical spectrums (W, R, G, B).
   B. Calculate cell spectrum from "Module" and "BLU" spectrums.
   C. Calculate color chromaticity by using cell spectrum and the spectrum of standard light source "C".
5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG4.

FIG.4 Viewing Angle



4. Interface Specification

4.1 Input power

The RX0275TA02.Open Cell Unit requir es power input which is emplo y ed to pow er the LCD electronics and to drive the TFT array and liquid crystal.

Item		Symbol	Min.	Typ.	Max	Unit	Note
Power Supply Input Voltage		V_{DD}	10.8	12	13.2	V	1
Power Supply Input Current	Black pattern	I_{DD}	-	0.34	0.41	A	2
	White pattern		-	0.36	0.43	A	
	H-strip pattern		-	0.5	0.6	A	
Power Consumption	Black pattern	P_C	-	4.08	4.92	Watt	
	White pattern		-	4.32	5.16	Watt	
	H-strip pattern		-	6	7.2	Watt	
Inrush Current		I_{RUSH}	--	--	4	A	3

Note1. The ripple voltage should be fewer than 10% of V_{DD} and min. V_{DD} (including ripple min.) must be over 10.8V at any time..

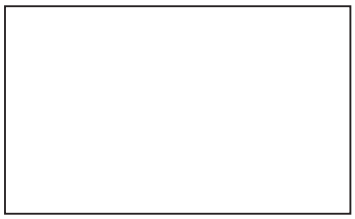
Note2. Test Condition:

(1) V_{DD} = 12V, (2) Fv = 60Hz, (3) Fclk= 74.25MHz, (4) Temperature = 25 ℃

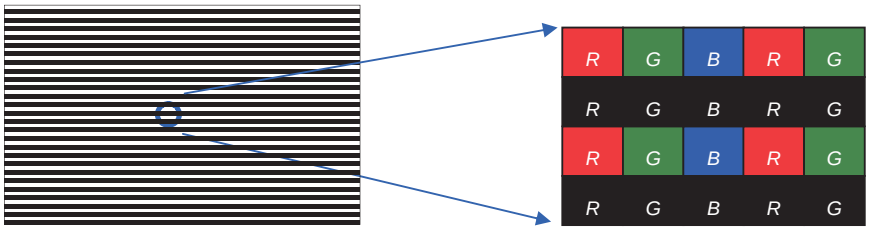
(5) Power dissipation check pattern. (Only for power design)

a. Black pattern

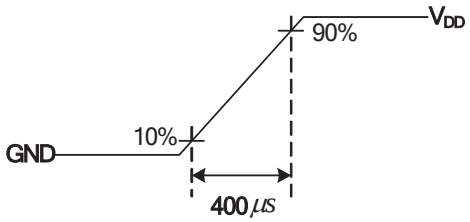
b. White pattern



c. H-Strip pattern



Note3. Measurement condition : Rising time = 400us

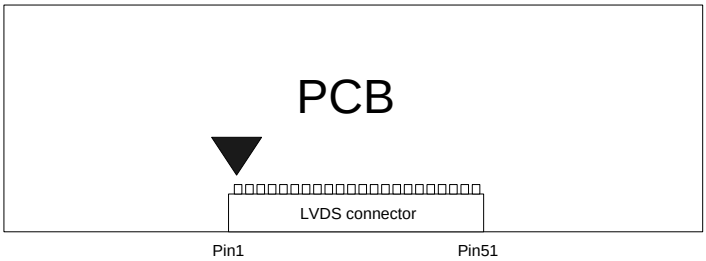


4.2 Input Connection

■ LCD connector: JAE FI-RTE51SZ-HF

PIN	Symbol	Description	Note	PIN	Symbol	Description	Note
1	N.C.	No Connection	2	26	GND or N.C.	Ground or No Connection	7
2	SCL	I2C Clock	3,4	27	N.C.	No Connection	2
3	WP	Write Protection	3,5	28	CH2_0-	LVDS Channel 2, Signal 0-	
4	SDA	I2C Data	3,4	29	CH2_0+	LVDS Channel 2, Signal 0+	
5	N.C.	No Connection	2	30	CH2_1-	LVDS Channel 2, Signal 1-	
6	N.C.	No Connection	2	31	CH2_1+	LVDS Channel 2, Signal 1+	
7	LVDS_SEL	LVDS data format selection	3,6	32	CH2_2-	LVDS Channel 2, Signal 2-	
8	N.C.	No Connection	2	33	CH2_2+	LVDS Channel 2, Signal 2+	
9	N.C.	No Connection	2	34	GND	Ground	
10	N.C.	No Connection	2	35	CH2_CLK-	LVDS Channel 2, Clock -	
11	GND	Ground		36	CH2_CLK+	LVDS Channel 2, Clock +	
12	CH1_0-	LVDS Channel 1, Signal 0-		37	GND	Ground	
13	CH1_0+	LVDS Channel 1, Signal 0+		38	CH2_3-	LVDS Channel 2, Signal 3-	
14	CH1_1-	LVDS Channel 1, Signal 1-		39	CH2_3+	LVDS Channel 2, Signal 3+	
15	CH1_1+	LVDS Channel 1, Signal 1+		40	N.C.	No Connection	2
16	CH1_2-	LVDS Channel 1, Signal 2-		41	N.C.	No Connection	2
17	CH1_2+	LVDS Channel 1, Signal 2+		42	GND	Ground	
18	GND	Ground		43	GND	Ground	
19	CH1_CLK-	LVDS Channel 1, Clock -		44	GND	Ground	
20	CH1_CLK+	LVDS Channel 1, Clock +		45	GND	Ground	
21	GND.	Ground		46	GND	Ground	
22	CH1_3-	LVDS Channel 1, Signal 3-		47	N.C.	No Connection	2
23	CH1_3+	LVDS Channel 1, Signal 3+		48	V_{DD}	Power Supply Input Voltage	
24	N.C.	No Connection	2	49	V_{DD}	Power Supply Input Voltage	
25	N.C.	No Connection	2	50	V_{DD}	Power Supply Input Voltage	
				51	V_{DD}	Power Supply Input Voltage	

Note1. Pin number start from the left side as the following figure.



Note2. Please leave this pin unoccupied. It can not be connected by any signal (Low/GND/High).

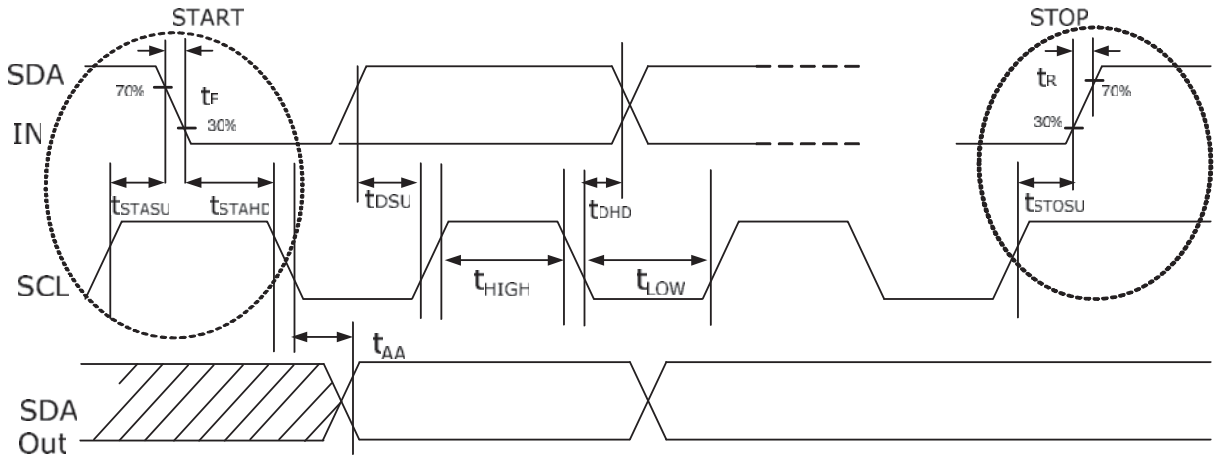
Note3. Input control signal threshold voltage definition

Item	Symbol	Min.	Typ.	Max.	Unit
Input High Threshold Voltage	VIH	2.7	-	3.6	V
Input Low Threshold Voltage	VIL	0	-	0.6	V

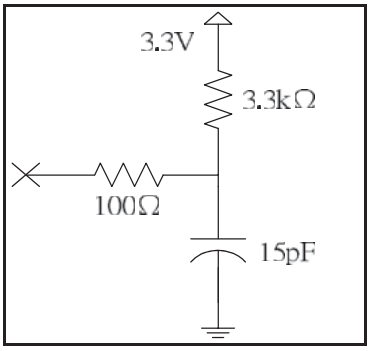
Note4. I2C Data and Clock

I2C Data and Clock timing

Parameter		Symbol	Min.	Typ.	Max	Unit
I2C	**SCL clock frequency**	**fSCL**	**-**	**-**	**350**	**kHz**
	Clock Pulse Width Low	**tLOW**	**1.85**	**-**	**-**	**us**
	Clock Pulse Width High	**tHIGH**	**0.4**	**-**	**-**	**us**
	Clock Low to Data Output Valid	**tAA**	**1.76**	**-**	**-**	**us**
	Start Setup Time	**tSTASU**	**0.6**	**-**	**-**	**us**
	Start Hold Time	**tSTAHD**	**0.6**	**-**	**-**	**us**
	Stop Setup Time	**tSTOSU**	**0.6**	**-**	**-**	**us**
	Data In Setup Time	**tDSU**	**0.1**	**-**	**-**	**us**
	Data In Hold Time	**tDHD**	**0**	**-**	**-**	**us**
	SCL/SDA Rise Time	**tR**	**-**	**-**	**0.3**	**us**
	SCL/SDA Fall Time	**tF**	**-**	**-**	**0.3**	**us**



Input equivalent impedance of SDA/SCL pin

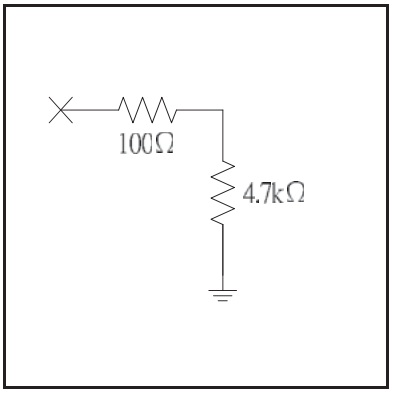


Note5. Write Protection

Mode selection

WP	Note
L or OPEN	Protection
H	Writable

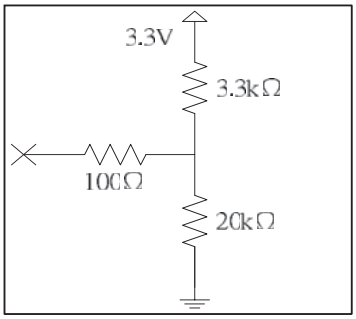
Input equivalent impedance of WP pin



Note6. LVDS data format selection

LVDS_SEL	Mode
H or OPEN	NS
L	Jeida

Input equivalent impedance of LVDE_SEL pin

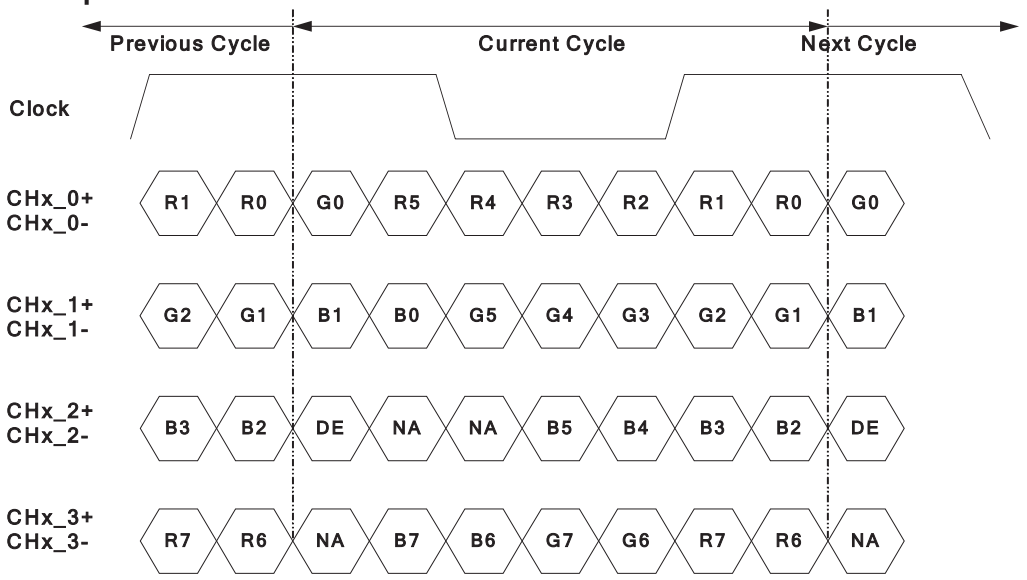


Note7. Please leave this pin unoccupied or connect to ground. It can not be connected by any signal (Low/High).

4.3 Input Data Format

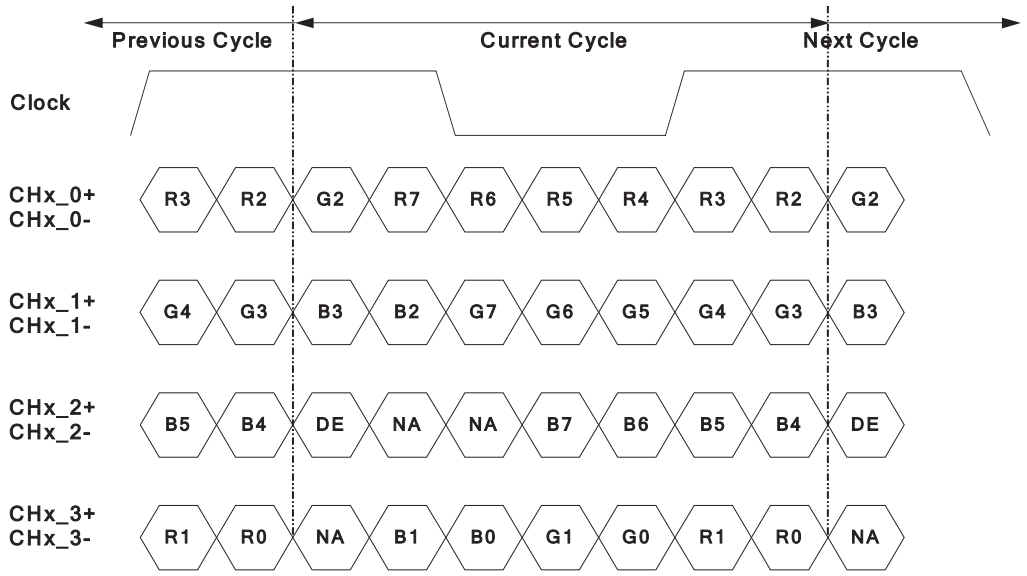
4.3.1 Data mapping

■ **LVDS Option NS**



Note: x = 1, 2, 3, 4…

■ **LVDS Option JEIDA**



Note: x = 1, 2, 3, 4…

4.3.2 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 8 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

Color		Input Color Data																							
		RED								GREEN								BLUE							
		MSB							LSB	MSB							LSB	MSB							LSB
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

4.4 Backlight Unit

Parameter		Min.	Typ.	Max.	Unit	Remarks
LED Light Bar Input Voltage Per Input Pin	VPIN	-	38.4	--	Duty 100%	
LED Light Bar Input Current Per Input Pin	I_{PIN}	-	259	--	mA	Note1,2,
LED Power Consumption	P_{BL}	-	9.95	--	W	Note 3
LED Life-Time	-	30,000	-		Hrs	Note 4

LED bar consists of 80 LED packages,2 strings(parallel)*(5 strings(parallel)*8packages(serial)

Note1: There are one light bar ,and the specified current is input LED chip 100% duty current

Note2: The sense current of each input pin is 140mA

Note3: PBL=2 Input pins*V_{PIN} ×I_{PIN}

Note4: The lifetime is determined as the time at which luminance of LED become 50% of the initial brightness or not normal lighting at IPIN=140mA on condition of continuous operating at 25 ±2 ℃

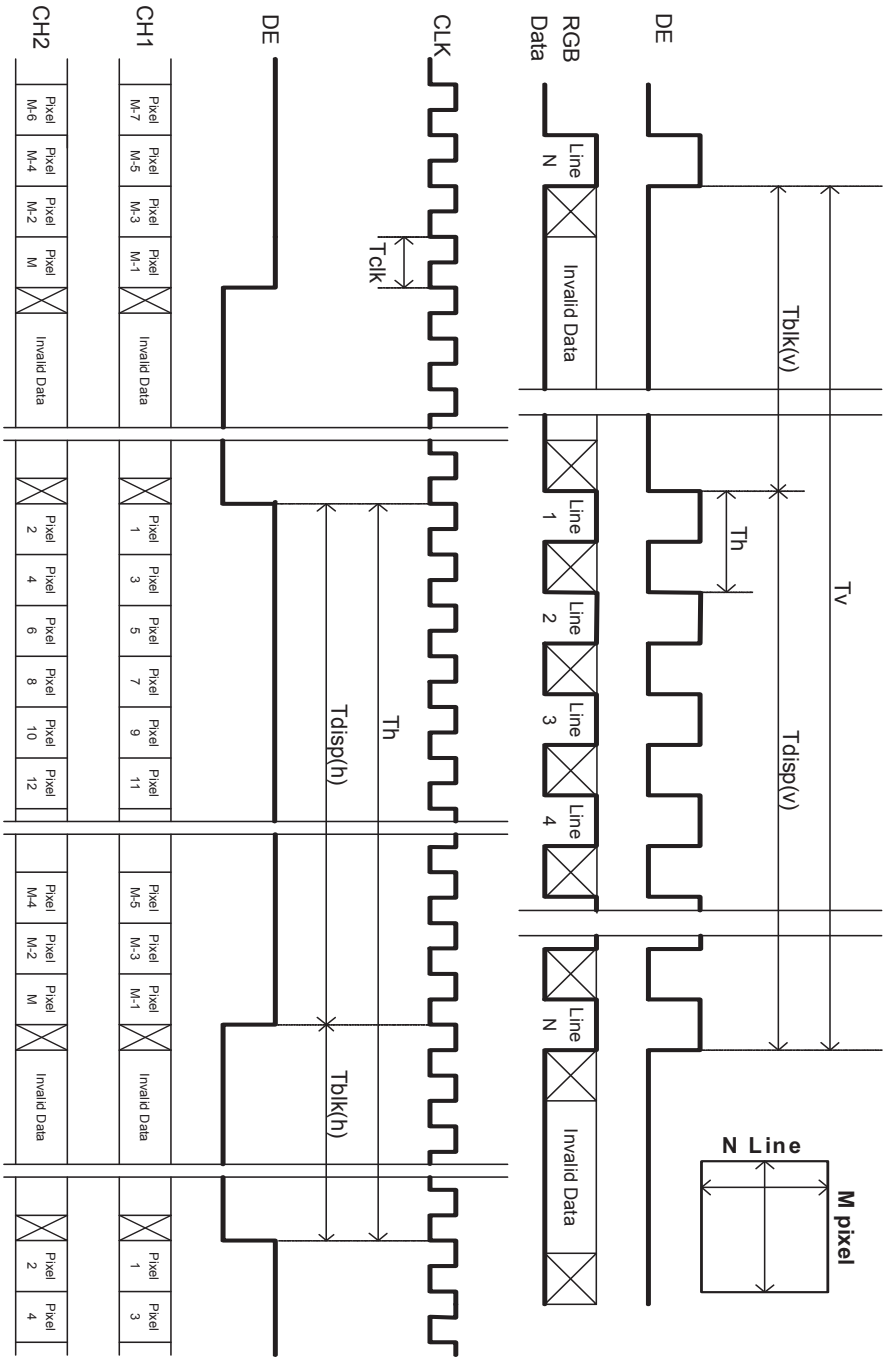
5. Signal Timing Specification

5.1 Input Timing

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

Timing Table (DE only Mode)

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	1100	1125	1480	Th
	Active	Tdisp (v)		1080		
	Blanking	Tblk (v)	20	45	400	Th
Horizontal Section	Period	Th	1030	1100	1325	Tclk
	Active	Tdisp (h)		960		
	Blanking	Tblk (h)	70	140	365	Tclk
Clock	Frequency	Fclk=1/Tclk	53	74.25	82	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	60	67.5	73	KHz



Note1. Display position is specific by the rise of DE signal only.
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.

Note2. Vertical display position is specified by the rise of DE after a “Low” level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen

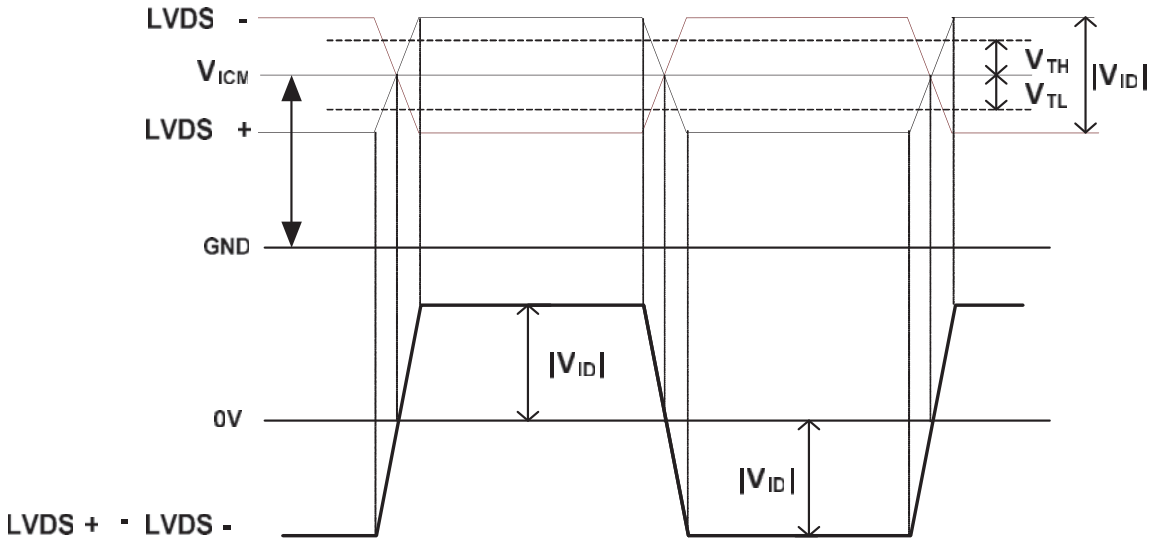
Note3. If a period of DE “High” is less than 1920 DCLK or less than 1080 lines, the rest of the screen displays black.

Note4. The display position does not fit to the screen if a period of DE “High” and the effective data period do not synchronize with each other.

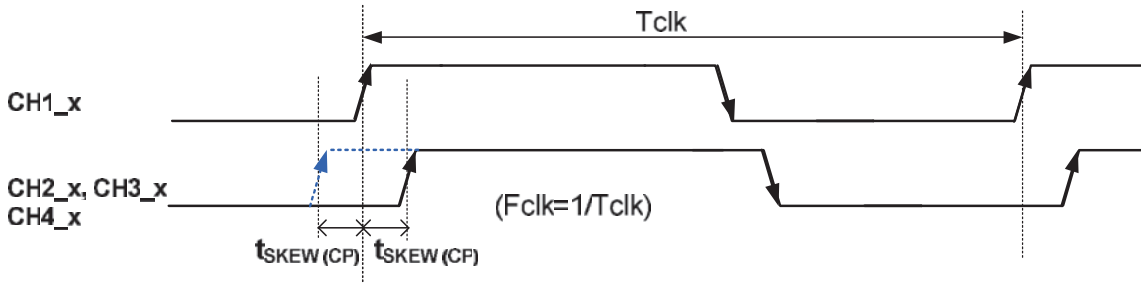
5.2 LVDS spec

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max		
LVDS Interface	Input Differential Voltage	$\lvert V_{ID} \rvert$	200	400	600	mV_{DC}	1
	Differential Input High Threshold Voltage	V_{TH}	+100	--	+300	mV_{DC}	1
	Differential Input Low Threshold Voltage	V_{TL}	-300	--	-100	mV_{DC}	1
	Input Common Mode Voltage	V_{ICM}	1.1	1.25	1.4	V_{DC}	1
	Input Channel Pair Skew Margin	$t_{SKEW\ (CP)}$	-500	--	+500	ps	2
	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -3%	--	Fclk +3%	MHz	3
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	30	--	200	KHz	3
	Receiver Data Input Margin Fclk = 85 MHz Fclk = 65 MHz	tRMG	 -0.4 -0.5	 -- --	 0.4 0.5	ns	4

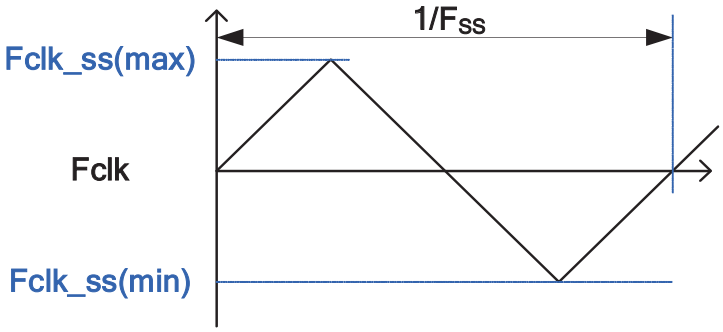
Note1. VICM = 1.25V



Note2. Input Channel Pair Skew Margin

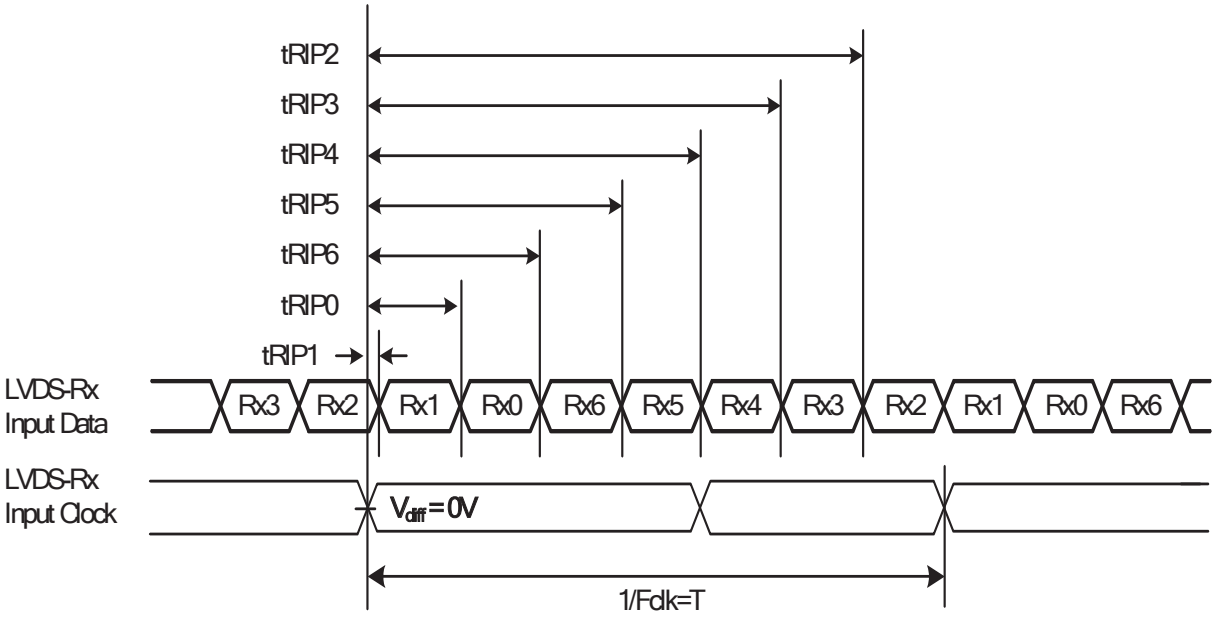


Note3. LVDS Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures.

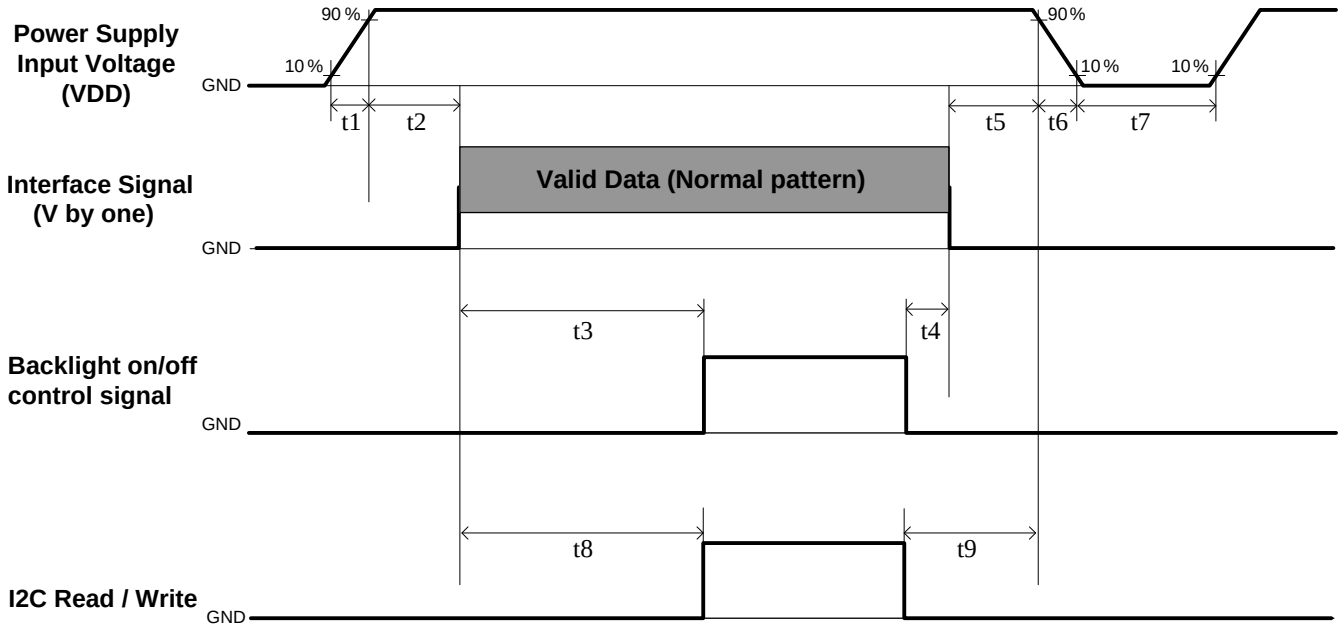


Note4. Receiver Data Input Margin

Parameter	Symbol	Rating			Unit	Note
		Min	Type	Max		
Input Clock Frequency	Fclk	Fclk (min)	--	Fclk (max)	MHz	**T=1/Fclk**
Input Data Position0	tRIP1	-|tRMG|	0	|tRMG|	ns	
Input Data Position1	tRIP0	T/7-|tRMG|	T/7	T/7+|tRMG|	ns	
Input Data Position2	tRIP6	2T/7-|tRMG|	2T/7	2T/7+|tRMG|	ns	
Input Data Position3	tRIP5	3T/7-|tRMG|	3T/7	3T/7+|tRMG|	ns	
Input Data Position4	tRIP4	4T/7-|tRMG|	4T/7	4T/7+|tRMG|	ns	
Input Data Position5	tRIP3	5T/7-|tRMG|	5T/7	5T/7+|tRMG|	ns	
Input Data Position6	tRIP2	6T/7-|tRMG|	6T/7	6T/7+|tRMG|	ns	



5.3 Power Sequence for LCD



Parameter	Min.	Typ.	Max	Unit
t1	0.4	---	30	ms
t2	40	---	---	ms
t3	640	---	---	ms
t4	0*1	---	---	ms
t5	0	---	---	ms
t6	---	---	---*2	ms
t7	1000*3	---	---	ms
T8	640	---	---	ms
T9	150	---	---	ms

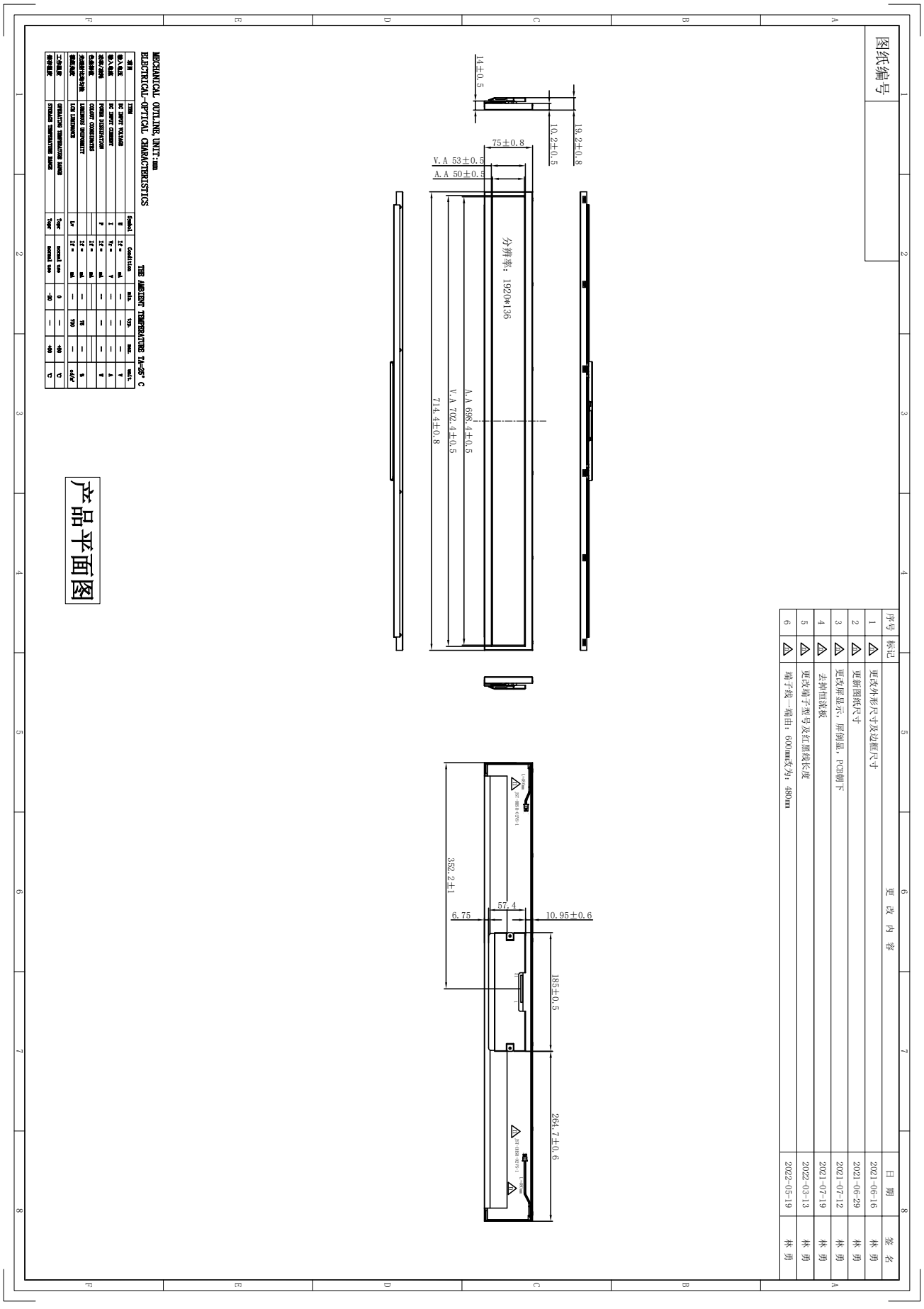
Note :

(1) t4=0 : concern for residual pattern before BLU turn off.

(2) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)

(3) When the power supply input voltage(VDD) is off, be sure to pull down the valid and the invalid data to 0V.

6. Mechanical Drawing



ITEM	Symbol	Condition	min.	typ.	max.	unit.
DC INPUT VOLTAGE	U	Ta= ℃	—	—	—	V
DC INPUT CURRENT	I	Ta= ℃	—	—	—	A
POWER DISSIPATION	P	Ta= ℃	—	—	—	W
CONTRAST CHARACTERISTIC		Ta= ℃	—	—	—	
LUMINANCE UNIFORMITY		Ta= ℃	75	—	—	%
LCD LIFETIME	Lbr	Ta= ℃	—	70K	—	cd/m²
OPERATING TEMPERATURE RANGE	Topr	ascend use	0	—	+60	℃
STORAGE TEMPERATURE RANGE	Tstr	ascend use	-20	—	+60	℃

7. Packing

TBD